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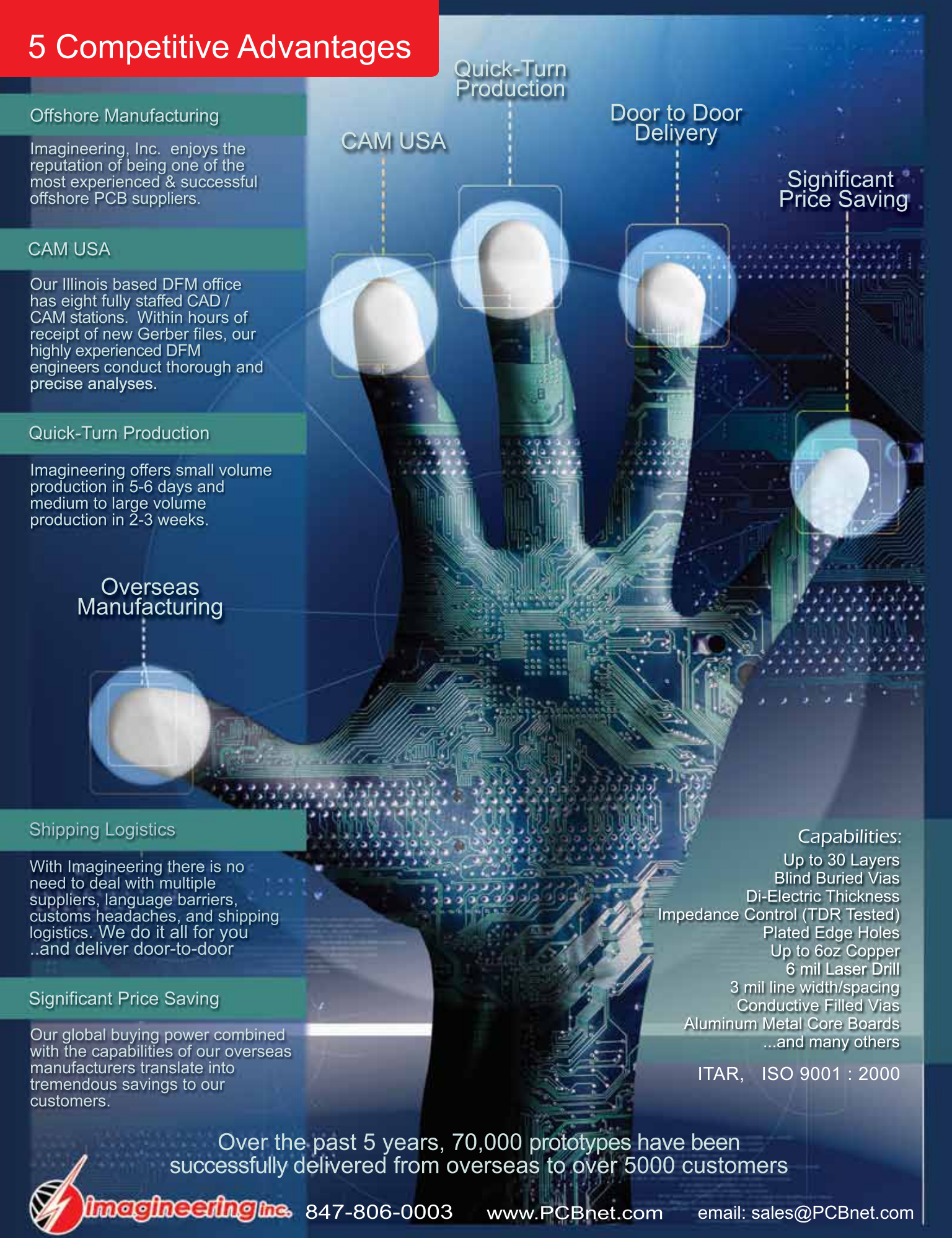

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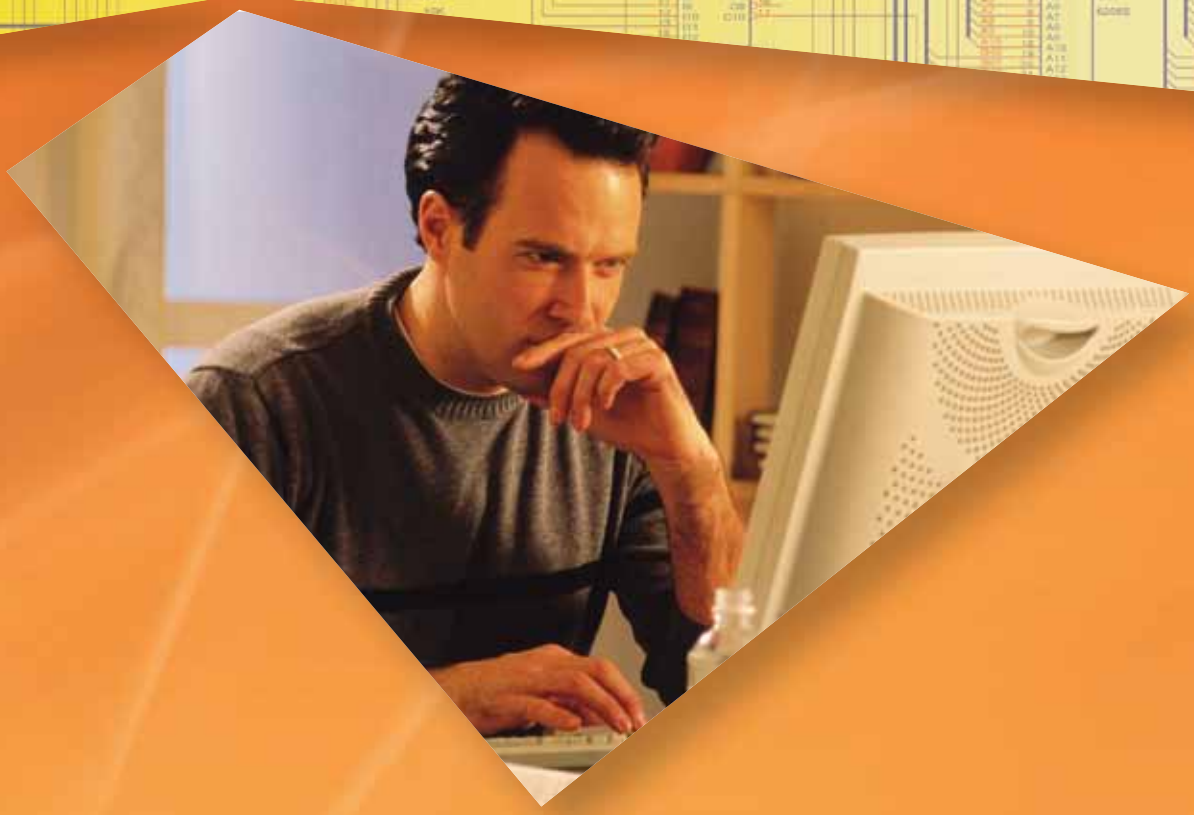

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MIKE BUETOW, EDITOR-IN-CHIEF

Mixed Appreciation for Depreciation

FOR SOME 15 years, the electronics manufacturing industry has pushed for changes to the US capital equipment depreciation laws.

In fits and starts, various groups have converged on Washington and lobbied legislators to shorten the five-year cycle for fully depreciating new machines, saying the move would make the US more competitive with other manufacturing-reliant nations. Most major electronics manufacturing countries permit one-to-three year depreciation schedules, boosting near-term cash flow, which is critical in a low-margin, materials-intensive business.

As communications director of IPC in the late 1990s, I myself spent untold hours running around the US Capitol, drenched from the summer heat and humidity, quietly gritting my teeth while listening to my colleagues get tongue-tied on what it is the industry does, while facing scads of lawmakers (or their prepubescent aides) less-than-eager to help their constituents. (Note to all would-be lobbyists: When a legislator says they support your issue but won't vote for it because they are waiting for an omnibus bill, they are lying.)

Thanks in part to 9/11 and subsequently in response to economic cycles, lawmakers have from time to time accelerated the schedule to three years and raised the amount small businesses could write off. But the US still trails its foreign competitors.

In October, President Obama offered full capital depreciation (and also said he would make permanent the much-sought-after research and development tax credit). Alone, this is terrific news for US businesses.

But Obama's plan comes with a catch: American businesses would no longer get tax breaks to launch operations offshore. "There is no reason why our tax code should actively reward them for creating jobs overseas," Obama said.

For US-based electronics companies, that's not so easy to swallow. Much of the supply chain exists happily offshore; bringing it back would not be impossible, but it's just not likely to happen.

The National Association of Manufacturers supports the accelerated depreciation laws (it would be hard to see why it wouldn't), but reportedly has come out against the other proposed changes to the tax code. As I'm sure NAM is aware, hits to the US Treasury must be made up elsewhere. Politics is the art of compromise and tradeoffs. I would urge our industry trade groups to collectively agree on what the electronics industry can afford to live with, and what it can't – and fast. They will be much more effective if they speak with a unified voice.

Thai'd down. The US isn't the only nation where business and lawmakers are locked in a struggle over the financial system. Thailand's government is considering a 21% hike in the minimum wage, leading several executives to warn that the move could push labor-intensive jobs elsewhere.

Thailand is home to several of the world's largest EMS firms, including Cal-Comp (no. 8 on the CIRCUITS ASSEMBLY Top 50), Team Precision (no. 19), Delta Electronics, Hana Microelectronics (no. 29) and SVI Public Co. (no. 47), not to mention no. 24 Fabrinet, which is based in San Francisco but whose factories are in Thailand.

We will hear more and more of this as Asia faces the same inevitable swell of worker pushback. Thailand suffers through massive worker strikes each year, and its government may finally be capitulating. With higher wages comes increased overhead, although it would take far more study and space than allowed here to examine whether the expenses related to training, turnover and (lower) end-product quality exceed those of a higher minimum wage.

What we do know, however, is that much of the world's economic model balances on the import economies of the US and Europe. Over time, this will have to change, lest we continue to endure sharp boom-bust cycles every few years.

Hot spots. We had a terrific PCB West show last month. Attendance was way up, and the energy was palpable. (See the recap starting on pg. 28.) We are grateful to our supporters, and have already made plans to return to Santa Clara in 2011.

About that editorial ... I heard from a reader who felt a reference in September's *Caveat Lector* to the suicides at Foxconn was in poor taste. My sincere apologies. Also, Jabil contacted me to clarify that my description of the EMS company's environmental database management is just a small part of its overall solution.

Retiring types. My old friends Karen McGee and Charla Gabert are retiring this fall. Through the years, both have been wonderful colleagues and even better friends. I wish them well.

Mike Buetow
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PCD&F People

Taiyo America appointed **Haruomi Yoshimoto** president, replacing **Dave Rund**. He joined the parent company in 1998.

National Instruments promoted **Alex Davern** to executive vice president and chief operating officer.

Epec Engineered Technologies has named **Kendall Paradise** president.

P. D. Circuits named **Frank Alberto** (pictured) vice president of quality and technology, and promoted **Andy D'Agostino** to vice president of operations.

Follow us on Twitter (@mikebuetow).

Umicore named **Robert Ziebart** Taiyo product manager.

San Francisco Circuits named **Vickie Duarte** global PCB engineer, responsible for front-end engineering, technical customer support and new business development.

PCD&F Briefs

FCI Microconnections (fciconnect.com) has opened a 234,000 sq. ft. flex circuit manufacturing facility, its third in Singapore.

The **World Intellectual Property Organization** has issued **AT&S** (ats.net) a pair of patents related to printed circuit fabrication: one covering a method and system for connecting multiple PCBs to at least one frame or carrier element, and PCB and frame or carrier element, the other relating to a method for monitoring the temperature-time-load of a PCB and/or at least one component on a PCB, using an irreversible color-changing time-temperature indicator (wipo.int/pctdb/en/ia.jsp?ia=AT2010/000067).

3M (mmm.com) has invested an undisclosed sum in **Printechnologics** (printechnologics.com), forming a joint venture for electronics circuits on paper or foil.

Rena-Hollmuller has named **M&M International** (mandminternationalinc.com) its representative for the Western US.

JX Nippon Mining & Metals (nmm.jx-group.co.jp) has named **Ticer Technologies** (ticertechnologies.com) its exclusive global manufacturer and marketer of TCR thin film resistor copper foil.

Ucamco (ucamco.com) named **Ascentech** (ascentechll.com) sales agent for the Northeast US.

Faraday Printed Circuits ordered a **Micro-Craft** (microcraft.com) MJP inkjet legend

DEVELOPING COUNTRIES TO DRIVE ELECTRONICS ECONOMY

LA QUINTA, CA – Electronics equipment growth will outpace worldwide GDP by a factor of more than two-to-one over the next five years, while PWB growth will be even higher, according to a leading industry analyst.

Real gross domestic product compound annual average growth from 2009 to 2014 will be 3.5% worldwide, 6.3% for emerging economies. Meanwhile, electronics equipment will experience a CAGR of 7.8%, and PWBs will have come in at 9.1%, says Henderson Ventures (hendersonventures.com). However, much of the PWB growth is already behind us: From 2010 to 2014, the PWB CAGR will be 6.9%, Henderson says.

North American PWB production this year will grow 11.6% year-over-year, then rise 2.4% and 5.2% in 2011 and 2012, respectively, says Ed Henderson, principal analyst. In Asia, PWB production will be up 19.1% this year compared to 2009. In 2011, it will grow 6.1%, and in 2012 PWB production will rise 9.7%.

World PWB production in 2009 was $44.2 billion. Between 2009 and 2014, the CAGR for PWB production will be 9.1%, but only 6.9% for the world's major industrial nations. "Developing countries will be the ultimate drivers of the economy," Henderson asserted.

Speaking at IPC Electronics Industry Executive Summit in October, Henderson said global gross domestic product will rise 3.7% in 2010, then 3.3% in 2011 and 3.8% in 2012. The rates are weak compared to historical norms of 4% or more, Henderson said. World GDP next year for developed nations will be up 1.9%, while emerging economies will see a rise of 6.1%.

Global equipment production in 2010 will be nearly $1.9 trillion, up from $1.62 trillion last year. Equipment growth will be 22.6% this year; 8.7% in 2011 and 7.5% in 2012. –*CD*

IPC Summit: 'Firms Cash Rich,' But Spending Slow

LA QUINTA, CA – The US recession ended in the summer of 2009. You hadn't noticed? That's because recovery has been "mediocre, muted," according to Shawn DuBravac, chief economist and director of research for the Consumer Electronics Association (ce.org).

DuBravac led off the IPC Electronics Industry Executive Summit in October, saying the recession, though over, has been followed by a slower recovery than in the past, especially with regard to wages. Not much growth this year has been from personal income, he said, which is merely "inching up." Yet with the holiday season still ahead, there's reason to be hopeful, especially for companies with new products in the pipeline.

The financial story is twofold. While companies are heavy on cash, they are hoarding their wealth. Meanwhile, individuals are strapped for cash, and most of their wages go toward living expenses and debt reduction.

Some 60% of technology companies' revenue is earned overseas, Dubravac says, and while firms are "cash rich," they aren't spending. For their part, "employees are capturing less corporate compensation than ever" – or what DuBravac calls "corporate GDP." Companies are doing well, but it's "not trickling down to employees."

Where recent income growth has been seen is in the area of government transfers such as unemployment and social security, he notes, representing 18% to 19% of total income – higher than any time in the past 30 years. The job market offers only a small glimmer of hope: It will continue to recover slowly, he says. Interestingly, technology is continuing to garner a greater share of the consumer spend.

After a strong first quarter for US technology growth in both units and revenue, the recovery "dissolved," DuBravac said, with a "mediocre summit" followed by

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TTM Technologies (ttmtech.com), the top supplier of printed circuit boards to the US Department of Defense, has approved an agreement under which two of its major shareholders would be prohibited from accessing classified military information.

MacDermid's Advanced Surface Finishing division (macdermid.com) has implemented a surcharge on selected products in Greater China.

CIRCUITS ASSEMBLY People

Plexus named **Steve Frisch** regional president, EMEA.

Dymax has appointed **Luis Kowalewski** sales manager, Europe.

PartnerTech named **Dan Turecek** executive vice president operations for systems integration and enclosures, and **Peter Nilsson** executive vice president operations for electronics. **Jan Johansson** has been promoted to executive vice president market & sales.

Zestron named **Sal Sparacino** technical marketing manager.

IEC Electronics promoted **Jeffrey T. Schlarbaum** to president and **Donald S. Doody** to executive vice president.

SMT International named **John Snyder** vice president, responsible for its Amtech solder line.

Sypris Electronics named **Jim Long** vice president of operations. He was vice president and general manager of Sanmina-SCI Optical Technology.

LaBarge has named **Jens Hauvn** director of corporate quality.

CIRCUITS ASSEMBLY Briefs

Danaher (danaher.com) has agreed to acquire **Keithley Instruments** (keithley.com) for approximately $300 million. Keithley's board has approved the purchase. The acquisition is subject to customary closing conditions.

Aqueous Technologies (aqueoustech.com) named **Restronics** (restronics.com) manufacturer's representative in IN, OH, Eastern MI, KY and Western PA.

AIM (aimsolder.com) named **G-Force Reps** (gforcereps.com) its representative for the complete line of electronic solders and

negative growth. A new recovery is just starting, and unit growth this year will amount to a few percentage points.

The biggest growth will be for tablet PCs, but they are starting from a low mark. Seven million tablets will be sold in 2010, and sales are set to double in 2011. Video game hardware is forecast to fall about 1% compared to 2009. However, in the fourth quarter, the CEA expects a "launch of new accessories [that] will extend the life of consoles by a year or two." Typically, video game hardware has a five-year cycle, but the current trend is closer to six to six-and-a-half years.

Digital camera revenue growth is exceeding unit growth, an "unusual" occurrence. TV unit growth has been mediocre, and inventory high, and something must give in the balance between stock levels and pricing. MP3 players are down 11% year-to-date compared to 2009. For 2010, they will be down about 8% year-over-year.

"3D TVs and tablets will easily see half their volume in the fourth quarter" this year, and "tablets will become the first and second quarter 2011 story," DuBravac says. New gaming accessories also will do well in the December quarter.

DuBravac believes half the annual volume of new technology comes in the fourth quarter, a phenomenon he calls the "50% Rule." Of total technology, new and old, 22% of annual volume is in the first quarter, and 27% is in the fourth quarter. *–CD*

Cal-Comp Enters US Market

SAN DIEGO – Cal-Comp, the world's sixth largest EMS company, has acquired Spectragraphics, the parent company of a pair of US-based EMS companies, for an undisclosed price. The deal is expected to close in the next 60 days.

Despite its size – Cal-Comp (calcomp.co.th) had sales of $3.3 billion last year – the acquisition marks Cal-Comp's entry in North America. The company is based in Thailand, where it also is publicly traded, and itself is a subsidiary of Taiwan's Kinpo.

As part of the acquisition, Cal-Comp will get EMS firms SMS Technologies (smstech.com), based in San Diego, and Total Electronics (totalems.com), which has factories in Logansport, IN, and Reynosa, Mexico.

Spectragraphics has revenue of roughly $60 million to $70 million a year, according to reports. All 400 workers will be offered their current jobs under Cal-Comp. *–MB*

Pb-Free Material Could Replace PZT in Electronics

LEEDS, UK – A group of UK researchers are showing the potential of a new synthetic material to replace Pb-based ceramics in electronics devices.

Materials engineers at the University of Leeds are investigating Pb-free ceramic materials that, in certain situations, can be substituted for traditional piezoelectric material such as lead zirconium titanate (PZT). The researchers assert a Pb-free ceramic known as potassium sodium bismuth titanate (KNBT) shows many of the necessary electrical and chemical properties of an adequate replacement for PZT. The researchers also claim KNBT is lightweight and usable at room temperature.

Their research was published in October in *Applied Physics Letters*.

Pb-bearing piezoelectrics are currently exempt under EU RoHS laws, but uncertainty looms over long-term exemptions of any Pb-based material. *–MB*

Suntron Shines in Rain

METHUEN, MA – Rain drizzling on their heads, a small army of state and local politicians were on hand as EMS firm Suntron (suntron.com) in October officially opened its manufacturing plant here north of Boston.

The company recently checked into the new 41,000 sq. ft. factory, consolidating two plants in Manchester, NH, and Lawrence, MA. The new site employs about 100

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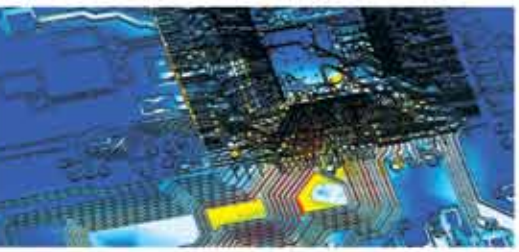

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chemicals in TX, OK, LA and AR, and **T & M Sales** (tmsales1.com) representative of its solders and chemicals in Delaware and Maryland.

Production Solutions (production-solutions.com) was awarded a patent for its Red-E-Set VB board support for screen printers with vacuum box tooling. It was issued to Douglas Farlow and Thomas Gordon. The patent number is 7,311,302.

Henkel (henkel.com/electronics) named **JSK Associates** representative in Northern CA and NV.

DEK (dek.com) and **AGI** have expanded their partnership with the addition of a stencil manufacturing facility in Tampa, FL.

Miele & Cie. (miele.de) has purchased a **Seho Systems** (seho.de) THT manufacturing line.

Yincae Advanced Materials (yincae.com) named **Cobar Europe** (cobar.com) distributor of its underfill and solder joint encapsulations in Europe.

SisTech Manufacturing (sistechmfg.com) installed a **Europlacer** (europlacer.com) iineo-II SMT machine.

Bulova Technologies' sale of its Melbourne, FL-based EMS unit should be complete by this month.

Saline Lectronics (lectronics.net) purchased a **Juki** (jukiamericas.com) FX-3 XL chipshooter.

MEC (meccompanies.com) added a **Mydata** (mydata.com) MY500 jet printer and MY100-DX14 placement machine, **Vitronics** (vitronics-soltec.com) XPM820 reflow oven and a **Yestech** (yestech-inc.com) BX-12 AOI to its Milwaukee plant.

Milara (milara-smt.com) named **Technica U.S.A.** (tecnicausa.com) to represent its line of screen printers for SMT and semiconductor manufacturing on the West Coast and Colorado, and **G-suit** (gsuit.co.il) as its representative in Israel.

Computrol (computrol.com) purchased an **Essemtec** (essemtec.com) Tucano screen printer.

Frontline Electronics (frontlineelectronics.com) installed a **CyberOptics** (cyberoptics.com) QX500 AAOI and SE350 SPI.

Nokia (nokia.com) will shutter its last manufacturing site in North America, sources say.

Flextronics (Flextronics.com) opened a one million sq. ft. computing facility in Wuzhong, its fourth in China.

workers, officials said.

Among those welcoming Suntron CEO Ed Wheeler to town were Massachusetts Lt. Governor Tim Murray, US Rep. Niki Tsongas (D-MA), Mayor William Manzi III and others. Wheeler addressed the company employees, visiting dignitaries and local press, saying that while "a lot of competitors are leaving the area," he believes "there are a lot of customers here to serve."

Inside, the facility, billed by the electronics manufacturer as "state of the art," was a bit long in the tooth insofar as equipment was concerned. The three SMT lines featured Speedline Ultraprint printers, two Siemens and four Mydata 15E placement machines and Heller 1800W reflow ovens. AOI is performed on an Agilent SP50, and x-ray on a new Dage XD7500VR. A pair of Electrovert Econopak wave machines occupied one corner. Because of the range and mix of customers, parts are kitted. The plant mostly uses no-clean, but some cleaning is performed using alcohol and a Trek aqueous cleaner. New to the site is a PVA automated conformal coater. One interesting sight was a portable Class 10,000 cleanroom.

Suntron VP of sales Roger White at the new EMS site.

According to vice president of sales Roger White, Suntron Northeast has between 28 and 32 customers on average, and its top seven customers make up about 60% of the site's sales. The plant builds for military, aerospace (it has AS9100 certification), medical, networking, semiconductor and industrial applications, among others. *–MB*

Report: Foxconn Employees Work Excessive OT

SHANGHAI – China state media in October issued a series of reports accusing Foxconn of forcing local staff to work excessive overtime and exploiting interns. The world's largest EMS company denies the charges.

University researchers surveyed 1,736 workers at the EMS company's factories in nine cities. They learned, per reports, that employees work an average 83.2 hours overtime monthly, more than twice the maximum 36 hours stipulated by Chinese law.

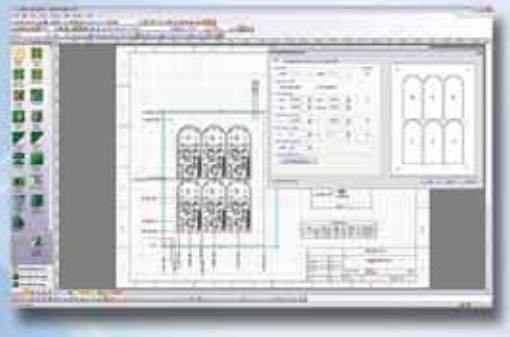
Survey results also showed workers claiming Foxconn cheated them out of overtime payments, while making interns work more than the legal eight-hour day. The firm is also accused of providing insufficient checkups for exposure to harmful substances, reports say.

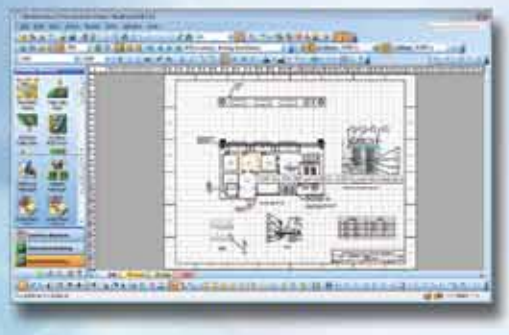
In a statement reported by Bloomberg, Foxconn extolled its commitment to a safe working environment and less dependence on overtime.

Foxconn has been under fire for low wages and the suicides of more than a dozen workers this year. *–MB*

NEW DIGS The applications lab at PVA's new 115,000 sq. ft. headquarters. The coating equipment OEM's lab handles R&D and customer trials.

BluePrint-4-Everyone





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DEFENSE DROPS

Trends in the U.S. electronics equipment market (shipments only).

	% CHANGE JUNE*	JULY[r]	AUGUST	YTD%
Computers and electronics products	-3.0	8.6	-2.1	12.3
Computers	1.7	3.5	7.1	13.9
Storage devices	-3.4	15.5	-0.8	26.3
Other peripheral equipment	2.8	3.6	-4.4	3.6
Nondefense communications equipment	-6.5	1.1	-0.5	-0.7
Defense communications equipment	-4.7	12.0	-14.6	-4.4
A/V equipment	12.4	-9.5	2.4	5.5
Components[1]	-1.0	5.2	-0.5	15.7
Nondefense search and navigation equipment	5.5	-8.3	1.5	-0.3
Defense search and navigation equipment	-4.2	-3.3	0.7	-1.4
Medical, measurement and control	-1.7	3.1	-1.8	19.5

[r]Revised. *Preliminary. [1]Includes semiconductors. Seasonally adjusted.
Source: U.S. Department of Commerce Census Bureau, Oct. 4, 2010

ISM: Overall Manufacturing Picture 'Less Encouraging'

TEMPE, AZ – Economic activity in the manufacturing sector expanded in September for the 14th consecutive month, says the Institute for Supply Management (ism.ws). However, the PMI fell 1.9 percentage points to 54.4%.

A reading above 50% indicates the manufacturing economy is generally expanding. However, the ISM went so far to point out that despite the positive PMI, many of the trend lines appear weaker. The PMI has fallen 11.5 percentage points from its January peak of 65.9%.

The overall economy grew for the 17th consecutive month, says ISM.

"While the headline number shows relative strength this month, the overall picture is less encouraging," said ISM spokesman Norbert J. Ore. "The growth of new orders continued to slow, as the index is down significantly from its cyclical high. Production is currently growing at a faster rate than new orders, but it typically lags and would be expected to weaken further in the fourth quarter. Manufacturing has enjoyed a stronger recovery than other sectors of the economy, but it appears that weaker growth is the expectation for the fourth quarter. Both the inventories and backlog of orders indexes are sending strong negative signals."

	MAY	JUNE	JULY	AUG.	SEPT.
PMI	60.4	59.7	56.2	55.5	56.3
New orders	65.7	65.7	58.5	53.5	53.1
Production	66.9	66.6	61.4	57.0	59.9
Inventories	49.4	45.6	45.8	50.2	51.4
Customer inventories	33.0	32.0	38.0	39.0	43.5
Backlogs	57.5	59.5	57.0	54.5	51.5

Sources: Institute for Supply Management, Oct. 1, 2010

METALS INDEX

DATE	10/5/09	7/5/10	8/2/10	9/6/10	10/4/10
LME Cash Seller and Settlement for Tin	$6.66	$7.82	$8.87	$9.69	$11.36
LME Cash Seller and Settlement for Lead	$0.95	$0.79	$0.91	$0.98	$1.03
Handy and Harman Silver (COMEX Silver)	$236.13	$260.41	$262.90	$290.11	$317.47
LME Cash Seller and Settlement for Copper	$2.66	$2.92	$3.27	$3.47	$3.68

Semi Forecast Lowered

EL SEGUNDO, CA – Saying consumer demand is slowing and inventories are rising, research firm iSuppli (isuppli.com) lowered its 2010 semiconductor revenue forecast to 32%, down from its previous outlook of 35.1%. Despite the reduced outlook, revenue will top $302 billion, up some $28 billion over the previous peak in 2007, iSuppli predicts.

iSuppli also lowered its forecast for fourth quarter sales, saying revenue will drop 0.3% sequentially, the first sequential drop in seven quarters. Still, iSuppli does not believe this signals the start of a significant downturn in the global semiconductor market. Global semiconductor revenue in 2011 will rise 5.1%, iSuppli predicts.

Meanwhile, The Information Network (theinformationnet.com) says indicators show a market correction is looming, with some signs pointing to a repeat of the correction that began after 2000.

Handset Sales Ring Up Big Gains

VANCOUVER – The number of mobile handset shipments is forecast to rise from 1.20 billion in 2009 to 1.43 billion in 2011, up 19.2%.

"We expect stronger growth over the next two years, especially in key Asian and African markets," said IE Market Research (iemarketresearch.com).

Equipment Outlook Mixed

LOS ALTOS, CA – Worldwide electronics equipment production will grow 13.3% this year, rebounding nicely following last year's 9.9% drop, according to new research from Henderson Ventures (hendersonventures.com).

Henderson forecasts output to expand 6.6% in 2011, then tick up to 7.3% in 2012 as commercial and industrial gains are partially offset by slumping military electronics demand.

INDUSTRY MARKET SNAPSHOT

Book-to-bills of various components/equipment.

	APR.	MAY	JUNE	JULY	AUG.
Semiconductor equipment[1]	1.13	1.13	1.18	1.23[r]	1.17[P]
Semiconductors[2]	50.4%	48.5%	42.6%	37%[r]	32.6%[P]
Rigid PCBs[3] (North America)	1.11	1.13	1.12	1.11	1.08
Flexible PCBs[3] (North America)	0.98	1.18	1.15	1.06	1.01
Computers/electronic products[4]	4.87	4.90	5.00	4.88[r]	4.90[P]

Sources: [1]SEMI, [2]SIA (3-month moving average growth), [3]IPC, [4]Census Bureau, [P]Preliminary, [r]Revised

The Rising Tide of the OEM Market

As influential as EMS and ODMs have become, the customer still drives the ship.

THOSE WHO FOLLOW our research know that we keep a close watch on the worldwide OEM electronics manufacturing market: in other words, the computer, communications, consumer, industrial/medical and transportation sectors. It is an enormous market in terms of revenue, reaching nearly $1 trillion in cost of goods sold (COGS) in 2008, before slipping to $832 billion in 2009. The recovery is expected to exceed $1.3 trillion by 2014 (TABLE 1).

What is remarkable about this market is its robustness. It is difficult to find markets of this scale expanding at the current compounded growth rate. Even more amazing, this growth rate has increased over the past few years with the explosion of notebook computer and mobile phones. Over the next five years, taking the lead will be consumer products: flat and 3D TVs, video game consoles, navigation systems and IP set-top boxes.

By comparison, the medical market always has exhibited solid growth, mainly in the areas of diagnostics and imaging systems, as well as surgical and monitoring equipment. Until last year, industrial product industries such as semiconductor capital equipment, process control, test and measurement steadily expanded. Yet with the downturn in 2009, capital spending went into a deep freeze and these markets contracted considerably. The same was true for automotive, although aerospace/defense and "other transportation" (off-road, trains, marine, etc.) remained relatively strong.

Nearly two-thirds of the OEM market today is comprised of computer and communications equipment, and this percentage is growing. A large part of these markets is commodity in nature, and once OEMs engage in the Asian business model of margin depletion, little money will be made from these sectors. Oddly, ODMs – e.g., Compal, Asus, Quanta, Wistron – (discussed later) last year were some of the most profitable in the industry. While EMS companies collectively lost $7 billion, ODM firms made more than $2 billion.

The real story behind the growth of the OEM market lies in where the assembly of electronics products is taking place. In this regard, we must look to EMS suppliers (including ODMs) and the growth rates associated with production taking place in low-cost countries. Today, EMS assembly accounts for around 32% of the total electronics assembly market. Yet, the growth of these suppliers in the three general low-cost regions (Mexico, Eastern Europe and China) account for the highest growth rates. Assembly value in these regions is approximately 50% higher than in high-cost regions (TABLE 2).

The reason behind this disruption can be understood when comparing the average base (unburdened) labor rates throughout the world. Essentially, an order of magnitude of difference exists between low-cost regions when compared to the base wage rate of high-cost regions. Making matters more difficult, once a competitor makes the move to migrate to a low-cost region, frequently others must follow to remain viable. (As the saying goes, "Once one cow crosses the rivers, so will the others.")

ODMs have disrupted the EMS industry the way EMS suppliers once disrupted the OEM electronics industry. ODMs typically have a lower cost of operation due to their focus on a select few commodity products and Asian (read: low cost) operations base. Moreover, they can discount assembly prices by raising design and component prices, which are often bundled into their service offering. As a result, EMS suppliers find it difficult to compete head-on with ODMs in the product sectors they excel in. FIGURE 1 highlights the supplier differences in value-add and cost.

OEMs like to work with ODMs because they lower risk by not having to invest in design, materials or inventory. (EMS companies frequently burden the OEM customer with inventory liability.) ODMs are attractive because they offer advanced designs,

TABLE 1. Electronics End-Market COGS, 2009-14

SEGMENT	2009	2014	CAGR
Computer	265.6	425	9.90%
Communications	197	304.7	9.10%
Consumer	167.2	273.3	10.30%
Industrial/Medical	93.9	142.5	8.80%
Transportation	108.5	164.9	8.70%
Total	832.2	1310.4	9.50%

Source: New Venture Research

TABLE 2. Regional EMS Growth, 2009-14

EMS MARKET	2009	2014	CAGR
Americas	47,519	84,424	12.20%
Mexico	15,056	27,348	12.70%
EMEA	38,105	66,713	11.90%
Eastern Europe	25,631	46,748	12.80%
APAC	184,070	327,728	12.20%
China	112,543	202,895	12.50%
Total	269,693	478,865	12.20%

In $millions. Source: New Venture Research

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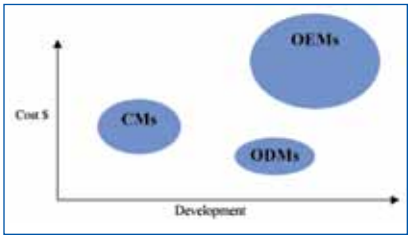

FIGURE 1. The cost-development relationship among ODMs, OEMs and EMS.

fresh IP and the ability to bring a new product to market very quickly. Where ODMs add risk is they may become a competitor once they gain the product design knowledge, as has happened in the past. Moreover, ODMs have a tendency to tolerate unhealthy profit margins just to gain a contract, and this can be risky for the OEM should the market soften or they go out of business. (Oddly Foxconn, officially an EMS company, succeeds by modeling an ODM business.)

With the EMS industry only accounting for 32% of the total available market, one might ask where is the other 68% of OEMs' product assembly? The answer can be found in the geography and business philosophy of leading electronics companies. By a wide margin, Asian (Chinese, Taiwanese, Korean and Japanese) OEMs prefer to manufacture in-house, while North American and increasingly European OEMs are looking to outsource as their business model. Further, a high percentage of OEM products simply are not able to be outsourced (aerospace, defense, medical, industrial, etc.) and are often produced in such low volumes that subcontracting is not profitable. As a result, EMS penetration is not expected to exceed more than 37% of the entire OEM industry by 2014.

NVR has analyzed the opportunity for outsourcing by market industry and leading OEM company in excruciating detail through its recent report, *The Worldwide OEM Electronics Assembly Market – A Unique Database Providing Global Electronics Assembly Data on Nearly 300 of the World's Leading Outsourcing Companies*, published in August 2010. For more information, see newventureresearch.com. CA

TABLE 3. 2009 EMS Labor Rates by Country

COUNTRY	HOURLY RATE (USD)
Germany	10.65
England	9.09
Japan	8.27
US	8.45
Ireland	7.86
Spain	6.21
Hungary	3.84
Mexico	2.35
Taiwan	2.7
India	1.3
China	1.22

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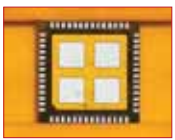

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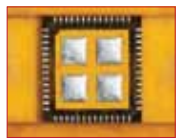
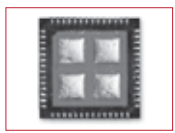


Step 3 - Reflow paste based on solder manufacturer's profile.



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The PCB Plateau

Stability has descended on the global industry, but for how long?

READING THE PRESS and listening to the news, it seems we have reached a plateau. The way I read the tea leaves, the number and rate of auctions within the industry has subsided and, due to a combination of dollar valuation, global economic activity and probably just dumb luck, terra firma has been attained by companies large and small.

Jeez, I hope I don't jinx things!

A plateau – a place where one can catch their breath and regain their footing – represents an opportunity. The opportunity is to set, or reset, your bearings, and in doing so, either "stay the course" you are on or set out on a challenging, if not exciting, new path. In either case the goal is to reach higher ground and not to slide backward – and the time is now!

Why is this the plateau and now the time? Simply because, for our industry, there is no region that currently has either a marked advantage or significant disadvantage. We appear to be on a level, if quirky, playing field, like a football field that looks flat but has enough divots to make a ball kick up in unexpected ways, or stop rolling for what appears to be no apparent reason. When playing on such a quirky field, it often can be mastered by changing how you play your game to take advantage of the inconsistency and all the questions that creates.

And what kinds of divots are on the field? With so much contraction in North America, weaker players are gone; what remains are companies with expertise, technology and tenacity. Ditto for Europe, where even fewer players are poised to supply technology and environmentally dynamic demand. In Asia, especially China, costs are rising and employee turnover is increasing from already historic highs – factors that, combined, raise serious questions regarding consistency and cost-effectiveness. The impact on buying has escalated over just a few quarters, with many now seeking alternatives. Meanwhile, the rest of the world is just that; no area has emerged as a potential game-changing, leading-edge threat.

In short, the paradigm shift taking place for over a decade appears to have stalled, albeit temporarily, with the result that globally, all parties are in a similar position of needing to take a deep breath, look around, and either confirm or reset strategic direction.

Taking advantage of the moment and reevaluating goals, directions and tactics is not easy. The opportunity for all is to build on what they have done well, while addressing the perceived or real weaknesses experienced. For those in North America, where the perception is that the highest technology is not available and everything is too expensive, the challenge is to demonstrate how to cost-effectively provide the highest technology. For Asia, where first-pass yield and quality are perceived to be less available than irrational pricing, the challenge is to demonstrate better quality and responsiveness. For those perceived to be limited by virtue of being "niche" or regionally focused, the challenge is to demonstrate ability to supply a variety of product across a wide geographic footprint.

Not all companies may want to make dramatic change, as many are successful "sticking to their knitting" and maintaining focus. If you are successful and believe your business can achieve higher plateaus, then you are on the right course, and you have confirmed your bearings. For those companies, this is the time to take a breath and re-commit your talent and treasure to the challenge of staying the course with as much vigor as possible.

However, many people and companies are not content. Some are still bitter that the "old order" of the last century radically changed, resulting in a lack of demand for same-old technology provided at less-competitive pricing. Others may have embraced change, but simply needed more time to accumulate the capital and talent to compete at the desired level. Still others may have experienced moderate success, but are not comfortable as to how long they can thrive on their current course. To those individuals and companies, now is the time!

Now is the time to look around and engage in making things happen. Now is the time to consult with suppliers, customers and employees to see what can be done better, faster, cheaper – either to enhance cost-effective delivery of technology or significantly improve service and quality performance. Now is the time to set the course and identify what is needed and how to reach the next plateau.

Testing the waters, asking the questions and setting the course – realistically – is never easy, but taking the required steps is. Begin by taking inventory of where you are, where your customers are, what resources you have and what resources you can reasonably expect to be able to muster as you progress. Then set a clear goal. From that goal, identify steps/actions to be made and the benchmarks that identify successful achievement of those tasks leading toward attaining the overall goal. And finally, set a timeline and get moving!

While the playing field appears level, be prepared for a lot of quirky sidesteps and pushback as the industry gains speed en route to the next plateau. The pause in velocity is now. However, as each company regains breath and footing, the opportunity to reconfirm or reset direction will quickly pass.

It's been a long time since the PCB industry has enjoyed such stability. Equally, we all have learned over the past decade that our market rewards those that are agile both strategically and tactically, and punishes those that remain internally focused and inflexible. I believe there is more opportunity – for everyone – than we have seen in a long, long time. PCD&F

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The Flexibility of Flex Circuits

The age-old technology is seeing new life in medical and other applications.

OLD TECHNOLOGIES NEVER die; they just get new names. Flex circuits have been around for many years in the IC packaging business and have been called almost as many names. In the early days, it was tape automated bonding (TAB). General Electric called it Mimi-Mod; Motorola called it Spider, and the first patent (despite an IP spat) was granted to a woman engineer, Frances Hugle, of Hugle Industries in 1969. TAB became famous with its use for driver ICs, connecting them to the ITO pattern on the glass LCD panel. The tape was Sn-plated, and issues with tin whiskers led Japanese companies such as Shindo Denshi to tackle the problem using an annealing process and nitrogen storage before bonding. Later the technology was called tape carrier package (TCP). Over time die were even mounted on the flex circuit without a bonding window, and the concept became chip-on-film (CoF).

In the 1980s, National Semiconductor licensed its TapePack technology to a several companies. This package also used TAB bonding. Kenzo Hatada at Matsushita developed a process called TB-TAB where a gold bump was placed on the TAB tape and die connected. Memory could be stacked this way. Other companies also worked on versions of stacked memory with flex circuits, including Thomson-CSF (now Thales). A 3-D package using flex is still in production today at 3D Plus, the spinoff from Thomson-CSP founded by Christian Val.

TCP was also used in Apple's Newton. LSI's ASIC was TAB-bonded in the package. The effort was the result of close cooperation among engineers with LSI, Sharp and Apple.

In the 1990s, flex became popular. A few ex-engineers (Tom DiStefano and Igor Khandros) from IBM got together and formed a company called IST. They came up with an idea to use flex circuit to make a really small chip-size package called a µBGA. They filed some patents, moved to California, and gave the company the name Tessera. Really, it was flex circuit. IC bond pads were connected to an array of bump connections on flex. Some DRAMs still ship in this type of package because this flex circuit structure provides excellent electrical performance. NEC developed a CSP using a flex circuit and called it a fine-pitch ball grid array (FPBGA). Nitto Denko used its ASMAT file with a z-axis conductive flex circuit material to form its Resin-Molded CSP. GE also applied its multichip module technology where flex was used for the redistribution layer to single-chip packages and called it a thin zero outline package.

Around 1995, Texas Instruments also came up with a CSP using flex circuit in order to make a low profile package called µSTAR BGA. This package is still in production. While these configurations were all single chip, flex circuit substrates were used for stacked die CSPs by Sharp, Fujitsu, NEC and many others because they provided an ultra-thin substrate that enabled a reduction in z-height. Tessera developed a folded, stacked package and Intel licensed it. This folder flex used a two-metal layer tape and was in production for many years until the business was sold to Marvell and the product reached end-of-life. Flex circuit substrate CSPs are being replaced by thin-core laminate substrates for new designs, but still accounted for approximately 1.5 billion packages in 2009.

Mainly driven by electrical performance, TAB tape was also used for large-size BGAs (TBGAs). Both TAB bonding and wire bonding have been used to interconnect pads on the die to flex circuit substrates. Semiconductor companies shipping TBGAs include Fujitsu, Freescale Semiconductor, NEC, Renesas and Toshiba. As rigid laminate materials have improved, TBGA volumes have declined.

While flex's popularity seems waning in some IC packaging applications, it is increasingly popular in medical electronics. Hearing aids, catheters, imaging systems, some implantable devices, and other products depend on flex to meet space, performance and density requirements. The digital hearing aid is a good example. Flex is often a folded product, and depending on the number of folds, the overall length of the flex can be more than 1.5 cm with one or multiple arms and a width of 5 to 10 mm (FIGURE 1).

Flex is expected to play an important role in wearable electronics. One of a number of research programs underway in Europe, TIPS is targeted at medical and health monitoring both for implanted and non-implanted medical devices, sensors, and portable and wearable electronics systems. A folded thin flex module containing a hearing aid flip-chip set has been demonstrated.[1]

Flex already is playing a role in the embedded component business for a multitude of applications. The Imbera technology, known as Integrated

(continued on p. 42)

E. JAN VARDAMAN is president of TechSearch International (techsearchinc.com); jan@techsearchinc.com. Her column appears bimonthly.

FIGURE 1. This hearing aid from Starkey Labs uses a flex circuit.

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When a Line Isn't a Line

Measuring differential pair loss requires both lines to calculate the attenuation.

WHETHER A HIGH-SPEED serial link channel works is just as dependent on the losses in the channel as its differential impedance. It's not enough to just meet an impedance spec and verify it using a test coupon. In many applications, it is also important to meet a loss spec and verify the attenuation of traces in a test coupon.

Measuring the signal-ended impedance of a trace in a test coupon is easy. All fab shops understand how to do this with a TDR. It is tempting to think that if you use the same line in a single-ended line or in a differential pair, a line is a line, and all you have to do is measure it once to know the differential impedance. After all, the other line in the pair isn't even touching its partner.

Unfortunately, while the proximity of the other trace in a differential pair will not change its single-ended impedance, the proximity will strongly affect the differential impedance of the pair.

Just measuring the single-ended impedance of one line in a differential pair, either as an isolated line or when in the differential pair, is no indication of the differential impedance. The measurement can be off by as much as 10% for tightly coupled microstrip or stripline pairs. You have to go the extra step to measure the differential impedance using a dual TDR.

Likewise, you cannot accurately measure the loss in a differential pair by just measuring the loss of one of the lines, or of an isolated version of that line. The coupling between the lines will affect the measured attenuation.

FIGURE 1 is a comparison of the differential insertion loss of a differential stripline pair, and of just one of the lines as a single-ended line stripline.

We usually define the losses in a uniform transmission line as the attenuation, measured in dB. Since the loss, in dB, increases linearly with the length of the line, it is often more common to use the metric of the attenuation per length, measured in dB/inch. For example, Intel recommends differential pairs used in PCIe III interconnects have a loss less than 0.78 dB/inch at 4 GHz.

In addition to geometry features, raw material and processing conditions will affect loss in a differential pair, making it necessary to measure test coupons to verify the attenuation per length of differential pairs on the board.

Unfortunately, measuring the attenuation of a single line that may be isolated or part of a differential pair will provide a different attenuation than the actual differential impedance of the pair. The coupling between the lines will affect the differential attenuation. Here's why:

Loss arises from conductor loss and dielectric loss. In stripline, attenuation from the dielectric loss is independent of coupling. If there were no conductor loss, measuring the attenuation of an isolated single-ended line or one line in a differential pair would give the same attenuation as the attenuation of the differential pair.

The attenuation from the conductor loss depends on the coupling in two ways. The attenuation is not due to just the series resistance alone, but the ratio of the series resistance to the differential impedance.

If the line width is kept fixed, and the two lines in a differential pair brought closer together, the differential impedance will decrease. Even if the series resistance were to remain constant, the attenuation would increase because the differential impedance decreased.

To complicate this further, the proximity of the two lines in the differential pair changes the current distribution in the conductors, changing the series resistance. Surprisingly, the series resistance goes down with tighter coupling as more of the return currents overlap and cancel. The current crowding in the signal traces does not start to increase the signal path series resistance until the spacing between the lines is much less than a line width.

The combination of these two effects means the attenuation will be higher in a differential pair than if measured as single-ended lines. This is all the more reason for all suppliers and users of high-speed differential channels to begin implementing a process to measure the attenuation of differential pairs for all high-performance boards. PCD&F

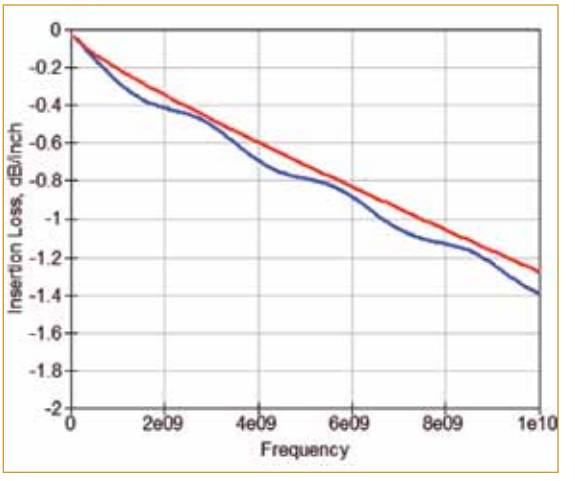

FIGURE 1. Comparison of differential insertion loss of a differential stripline pair and a single-ended line stripline.

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Creating Chip CAD Library Parts Smaller than 1608

How to interpret IPC-7351B for subminiature components.

AS COMPONENTS SHRINK, PCBs must be adjusted to compensate, or problems will occur. Among those issues is tombstoning, and here we look at possible solutions for assembly attachment of 0603 (EIA 0201) chip components.

IPC-7351B has a different set of rules for components smaller than 1.6 x 0.8 mm: namely, to adjust the land pattern to prevent tombstoning. But IPC-7351B also supports a three-tier environment system that includes "Least, Nominal and Most" land pattern sizes. The IPC-7351B mathematical model for land (pad) size and spacing calculations considers these tolerances the same for parts both larger and smaller than 1.6 x 0.8 mm. The final land size and spacing must compensate for the component body, terminal, and fabrication and assembly.

Gullwing, J-lead, wrap-around and L-bend component lead forms have a toe, heel and side solder joint goal. These values also are refined for large and small parts and large- and fine-pitch components. The component has a wrap-around lead.

There are also round-offs for the land size and land snap grid. For parts 1.6 x 0.8 mm and larger, the land size round-off is 0.05 mm and the land snap grid is 0.1 mm. For parts smaller than 1.6 x 0.8 mm, the land size round-off is 0.01 mm and the land snap grid is 0.2 mm.

IPC-7351B segments chip components as follows (TABLE 1):

- Component sizes of smaller than 1.6 x 0.8 mm, and equal to or larger than 1.6 x 0.8 mm.
- Solder joint goals of toe, heel and side.
- Environments of Least, Nominal and Most.

To calculate the land size and spacing of a component, the following are considered:

- Component body tolerance.
- Component lead tolerance.
- Fabrication and assembly tolerance.
- IPC three-tier environment solder joint goals (toe, heel and side).
- Small component or large component (the rules change).
- Land size round-off.
- Land placement round-off.

Take an average 1005 (EIA 0402) package. The body length is 1.0 x 0.5 mm with a tolerance of 0.15 mm. The terminal is 0.25 mm with a tolerance of 0.15 mm. This makes the minimum terminal size 0.1 mm and the maximum terminal size 0.4 mm. If the IPC-7351B mathematical formula for land size calculations compensates for this terminal tolerance range, the pad length will be 0.05 mm larger than if the terminal tolerance was 0.00 mm and both minimum and maximum terminal sizes were 0.25 mm. So my recommendation for chip parts "smaller" than 1.6 x 0.8 mm is never to enter the terminal tolerance into the IPC LP Calculator; i.e., keep the terminal size nominal for both the minimum and maximum dimensions.

Let's get real on this issue. A 1005 (EIA 0402) chip resistor with a minimum terminal of 0.1 mm (0.004") is an unacceptable feature size and unrealistic. And the 0.4 mm maximum terminal size would leave a 0.2 mm (0.008") gap between the terminals, also unrealistic. I don't believe any component manufacturer would actually deliver component terminal tolerances in this range, even though it's clearly printed in their datasheets. We must use common sense, especially with micro-miniature components.

Now, when the chip component goes below 1005 (EIA 0402) size, like the 0603 (EIA 0201), my recommendation is to use the IPC-7351B "Least" environment (FIGURE 1). The 0603 (EIA 0201) component is so small that it is in a class of its own. Also, to prevent tombstoning I highly recommend a "rounded

(continued on p. 48)

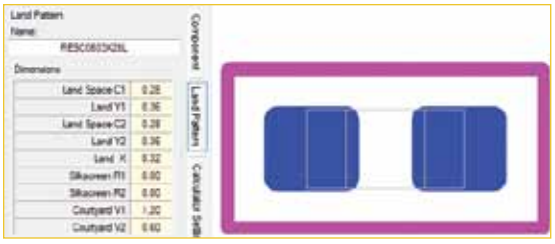

FIGURE 1. Least environment dimensions.

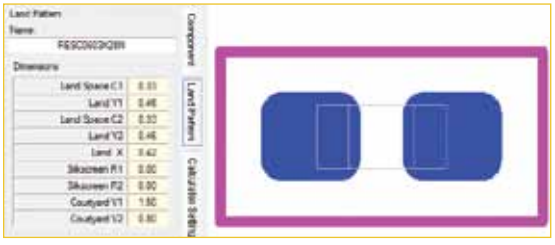

FIGURE 2. Nominal environment dimensions.

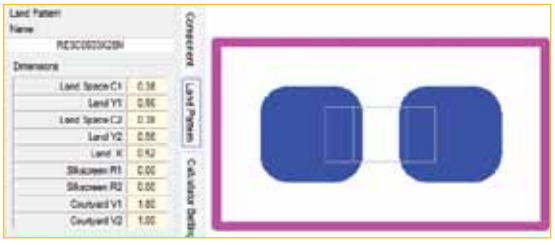

FIGURE 3. Most environment dimensions.

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Generalized I/O Timing Analysis, PART 2

The second of a two-part series looks at how timing and PCB trace lengths affect different real systems, and design tricks for tuning timing. by ISTVAN NAGY

On topology diagrams, we can easily visualize or specify the delays between any driver/receiver pair on multi-point nets. Some standards specify PCB design rules this way, for example, DDR-SDRAM DIMM memories (various Jedec JESD21-C documents) or Chipset Design Guides. Some design programs specify the constraints on these diagrams, like the Cadence Allegro Signal Explorer. The topology may be defined graphically, or as a spreadsheet for the point-to-point min./max. or relative length rules.[12]

Add-in cards: If a bus is routed through multiple boards, then the timing and length rules have to be correct for the whole system together (FIGURE 20). If different individuals or companies design the boards, they have to agree in the way of dividing the constraints between the boards, as a form-factor standard. In case of a clock tree, if the add-in card clock trace length is closely the same for all cards, then the skew can be controlled only by the motherboard design.

To control the ref./data signal arrival times at the capture flip-flop, control the delays on PCB traces. If two signals have similar drivers and trace lengths (matched), then the propagation delay and the transition delay also will be very similar, and propagation delay matching ensured by simple trace length matching.

The PLL (Phase-Locked Loop, on-chip device) can be used on continuously running clocks to introduce phase delays, negative delays or frequency multiplication. PLLs usually contain some kind of modifier element in their feedback loop. If this modifier element is a frequency divider (by M), then the PLL will generate an output clock, which has a frequency of M*f_in. If the modifier is a ΔΦ phase delay element, then the PLL inputs will be ΔΦ delayed from the output, so the output will be 360°- ΔΦ delayed from the input. If we have a PCB trace as the modifier element, then it will cause the inputs to be late by t_pd comparing to the output, so it looks like if the output was delayed by –1*t_pd from the input.

The DLL (Delay Locked Loop, on-chip device) is a fixed or adjustable delay element. It has "taps"; each tap has a unit delay value. The number of taps connected into the signal path determines the DLL delay.

To maintain the best timing for all on-chip data paths, the chips contain clock networks as balanced trees, so the clock will arrive to each flip-flop within a tight t_pd range. Normally there is an option to place a PLL before the clock tree to achieve zero clock propagation delay through the clock network. In some I/O applications, it might be useful, for example, if the clock network delay is a lot longer than the data path delay.

On bidirectional buses, minimize the clock skew between all the chips. If the clock is generated inside one of the chips,

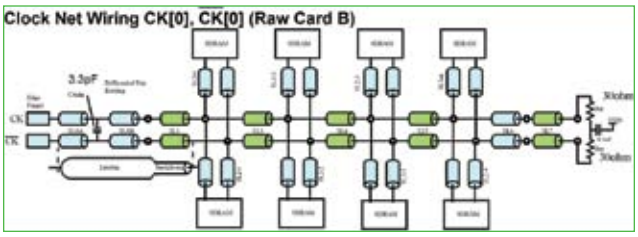

FIGURE 19. Fly-by clock net topology for one of the standard DDR3 DIMM designs from the JESD21-C standard. The ACC bus has similar topology, so the design ensures the clock-to-ACC timing as well.

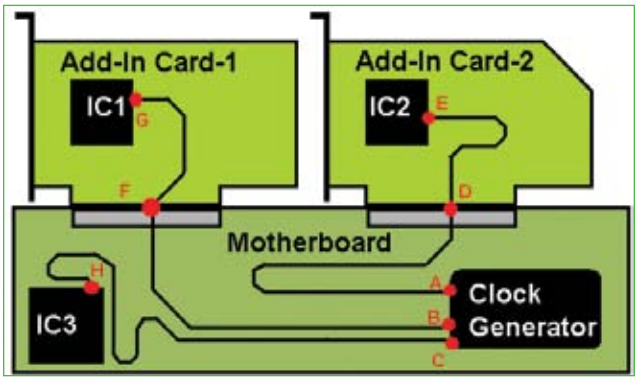

FIGURE 20. Add-in card routing example. The interface requires clock matching as A-E=B-G=C-H with some tolerance. To achieve this, the following routing rules apply: D-E=F-G (this is the rule for add-in cards), and A-D=B-F and C-H is longer than A-D by E-D (this is the motherboard design rule).

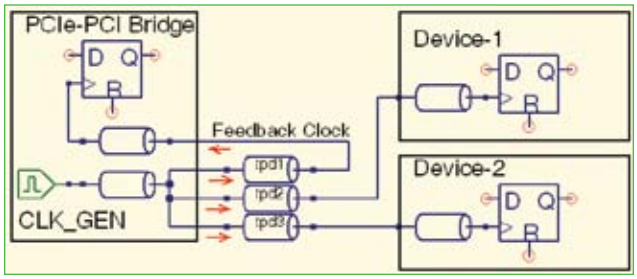

FIGURE 21. Using a feedback clock. t_pd1, t_pd2 and t_pd3 are matched.

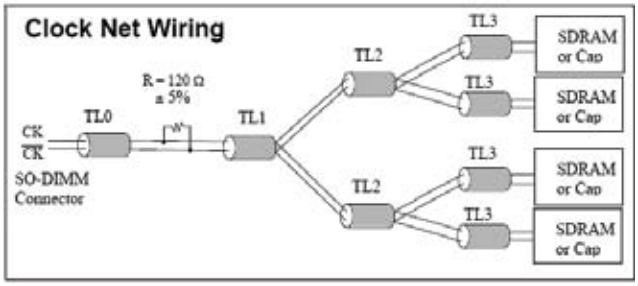

FIGURE 22. DDR-1/2 DIMM balanced tree clock (also ACC) topology.

then the clock propagation delay to that chip would be zero, while to the other chips it would be based on the on-board routing. To avoid that, we introduce the same clock propagation delay to the chip generating the clock, by using the feedback clock. This simply routes the clock back to the same chip. A data path with a certain delay in it can be divided into two separate paths by inserting a register or flip-flop into it. Both parts will have the same available time for signal propagation as the original path had, but with only a part of the original delay. Note that the data will arrive one bit time or one clock cycle later to the final capture flip-flop, but it will be captured with better timing margins. This technique is usually used on high-speed on-chip data processing, and on registered DIMM (RDIMM) memory card designs.

Usually the DLL/PLL delays are controllable, and we can also insert register stages in the datapath. These can be fixed by chip design or can be software programmable, but in most of the cases, they are adjusted automatically by a state machine. Examples are the DDR3-SDRAM memory Read and Write Leveling features.[2]

On-Chip Timing Design

Some of the above methods are really chip-design methods. The chip or ASIC/FPGA designers have to design their I/O interfaces to be operational with realistic board design. To achieve this, they set up timing constraints, use guided logic placement or floorplanning, do careful chip pinout design, use DLLs/PLLs, use localized high-speed IO clock networks, use asynchronous FIFOs and design clever architecture for backend data paths.[8,11,13]

The different devices in synchronous systems use the same clock source to run their I/O and on-chip flip-flops. There is always one clock generator, and its output is distributed to every device on the same bus. If the bus is bidirectional, then the best way to balance the read/write setup/hold margins is to balance/match the clock propagation delays. If there is a clock skew between two chips, then one of the margins is decreased by the value of the clock skew. The clock skew may be known as uncertainty (peak to peak), or as an absolute value (with a sign).

DDR-SDRAM memory interfaces have source-synchronous data buses (lanes), and they have a unidirectional synchronous address/command/control (ACC) bus. We have two types of implementations: the DIMM socketed card, and the Memory-Down, where the chips are soldered onto the motherboard. Either designing a DIMM card or a memdown, we usually follow the layout design rules specified in the appropriate card type from the JEDEC JESD21-C standard.[2, 9, 12]

The data bus timing is valid in every lane separately between the DQ/DM and DQS strobe signals. The DQS path has a DLL delay in the memory controller chip, so the DQS is delayed before entering to the PCB for write transactions, while for reads it is delayed only after it has arrived onto the controller chip.

The address/command/control (ACC) bus is sampled by the memory chips at the rising edges of the clock signal provided by the memory controller. In case of 2T clocking mode, every second rising edge is used to sample the ACC bus. The ACC bus is routed to every memory chip in a memory channel, so it can have a very heavy loading, which creates very slow transition delays. If the load is above a certain value, then we need registered/buffered DIMM memories. DDR1 and DDR2 standards use balanced-tree clock/ACC topology to make sure all chips get the clock/ACC in the same time, while DDR3 uses the Fly-By topology to minimize SNN and to have only one end where we can terminate them.

Reference-Reference Timing

Although the main I/O matching is between the data-strobe and the clock-ACC, there are also clock-to-strobe design rules. These are based on the chip timing design behind the I/O flip-flops.

The memory chips expect the first valid databit to arrive a certain time after they have captured a write command. The controller puts the first databit to the bus with the right timing, but the board design has to make sure that this timing is still maintained when the signals arrive to the memory. This requires a length matching between the clock and the strobe signals. For this, there is an output guaranteed skew timing parameter from the controller data sheet, and an input maximum skew parameter from the memory chip data sheet. This input parameter of the memory is the t_DQSS, which is +/- t_clk/4, between the rising edge of the clock and the rising edge of the DQS signal. They also specify a clk-rising to DQS-falling-edge input rule, which is the t_DSS and the t_DSH parameters together. For DDR3 memories, the write leveling feature can compensate for this.

The memory controller has to pass the captured data from the DQS clock domain to the internal clock domain. This clock domain crossing requires the data to arrive to the controller within a specified time window. This limits the maximum length of the bus, since if the bus is longer, then the data arrives later, decreasing the setup margin in the backend flip-flops. The memory chip data sheet specifies the maximum skew between the input clock and the output DQS, as t_DQSCK. The controller data sheet specifies a maximum skew of the output clock and the input. Both the clock and the DQS trace lengths increase this.

$$t\_sk\_in\_max \geq t\_DQSCK + t\_pd\_clk + t\_pd\_DQS + \sum_m t\_err_m$$

Some FPGA implementations handle this by calibrating the delay with DLLs and registers for all the read DQ/DQS signals.[9]

Timing calibration. We can include delay circuits in the DQ/DQS paths. These can be fixed, or adjusted by a hardware state machine or by software to achieve optimal timing. For example, if we extend the delay of a reference signal to t_clk, then the effect is like if the reference signal was not delayed at all (in the aspect of STA), although the controller has to expect the data in the next cycle (in the aspect of protocol). The board/chip delays are mostly static for a given board, although they vary between boards and over temperature. That is why we calibrate after power-up. We can measure signal quality by adjusting DLL delays step-by-step, capturing the data and seeking for the DLL value where the captured data is different than in the previous step. This way we can find the boundaries of the Data Valid Window. Then we can set the final delays in the middle of the region.

Write leveling. This process compensates for the clock-to-strobe matching issues, and skew caused by the fly-by ACC topology. The controller puts the memory chips into write leveling mode. Then the memory will sample the CLK using DQS edges; then it sends the captured value to the controller on the DQ0 line. The controller finds the two DLL values where the sampled value changes, then sets the DLL half way.

Read leveling. This process balances the data bus read setup/hold margins by adjusting the DQS delay. In read leveling mode, the controller writes a fixed test pattern into the general purpose register in the memory, reads it back again and again, seeking for the minimum and maximum delays where it can still read the correct data. Then it sets the DLL half way.

All DQ/DQS DLL calibration: FPGA-based memory controller implementations can have a separate DLL on each data line. This way we can compensate on-chip for board/chip mismatch.[9]

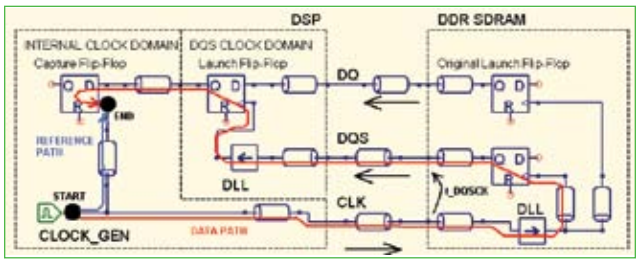

FIGURE 23. DDR memory Read data capture. After the data are captured from the bus by the DQS (primary loop), they are launched to the backend capture flip-flop in the internal clock domain (secondary loop).

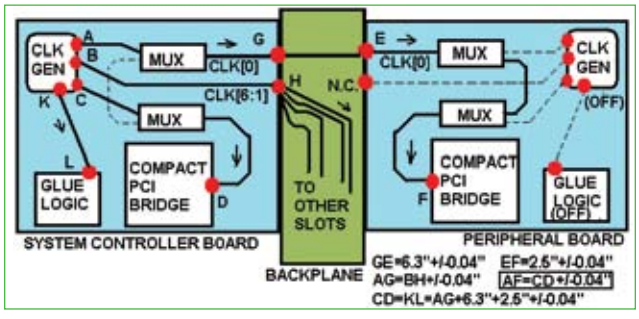

FIGURE 24. Compact PCI clocking.

Arbitrary examples. In Compact-PCI systems, a single board computer may be in a system controller or in a peripheral slot. In system controller mode, it has to supply the clocks to all other cards, and in peripheral mode, it has to take the clock from the backplane to clock its backplane I/O circuits. In both cases the clock signals have to be matched with a given tolerance. The system controller slot has 3 to 7 clock output signals, each routed to a different peripheral slot on the backplane with a length of 6.3"+/-0.04". The peripheral cards have to route this clock to their backplane interface circuits with 2.5"+/-0.04" length.

The MB86065 D/A Converter from Fujitsu receives the data as LVDS differential signals from the host (e.g an FPGA), and provides the I/O bit clock to the host. The DAC requires the data and the clock to be in phase + 90° at the DAC pins. The trick is to use a PLL feedback net on the PCB with a delay equal to the clock+data length on the PCB, creating a negative delay for the launch flip-flop. The PLL needs to have a 0° and a 90° output: the 0° for the feedback loop, and the 90° for the launch flip-flop for the extra alignment. This interface is a unidirectional synchronous interface, but the clock is provided by the receiver chip.[14]

When multiple lanes are used in the high-speed serial interfaces, in the receiver chip each lane has its own CDR (Clock-Data-Recovery) circuit, so each lane's SerDes will clock its parallel output with a different clock. These have a phase relationship based on the lane-to-lane skew on-board and on-chip. The parallel data are passed to the core clock domain. If that clock domain is derived, for example, from Lane-0 clock, then it will capture the Lane-0 parallel data with proper timing, but the other lanes will be early/late by the lane-to-lane skew. This is usually handled by a clock-DLL for lower speeds or by using asynchronous FIFOs for each lane. In case of a DLL, the max lane-to-lane skew is defined by STA at the clock domain crossing. In case of FIFOs, the maximum lane-to-lane skew is limited by the FIFO depth and the protocol. Some protocols define FIFO under/overflow control by transmitting align characters. The max skew can be t_skew < N * k * t_bit_serial, where they use "k" bits per symbol, and "N" is half the portion of FIFO depth allocated for deskew.[12]

Calculating PCB Trace Length Constraints

Trace length constraints can be calculated from the timing margins of the pre-layout timing analysis. These constraints are specified to ensure certain propagation delays. For multipoint buses, define pin-to-pin delay rules, or rules for "all pin pairs." Sometimes the signal travels through a series element: for example, a damping resistor or an AC coupling capacitor. The design program has to be able to measure the pin-to-pin lengths even in these cases.

Specify min./max. absolute or relative (matching) trace propagation delay or trace length rules, depending on the interface type. For the absolute data signal lengths, consider an already specified (by floorplanning) or routed reference signal length. Matching rules cannot be used for them, since the matching offset+tolerance would depend on the reference signal's length. The relative constraints for data signals specify trace length difference from the reference signal. For them, the reference length

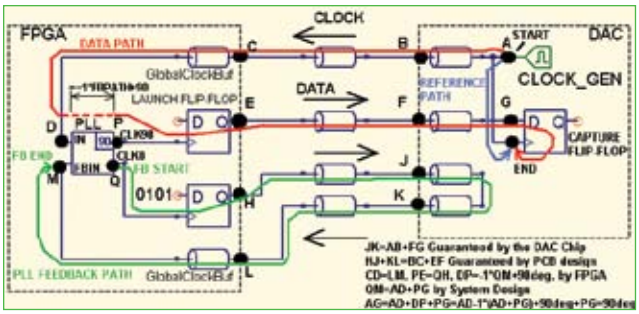

FIGURE 25. FPGA and MB86065 DAC interface timing.

need not be specified in advance.

The min./max. data propagation delay can be derived directly from timing margins, since the margins have been calculated using t_pd_data = 0 for absolute rules, or delta_t_pd = 0 for relative rules. Transform the smaller of the RD/WR margins to t_pd by checking what would cause zero margin. If the t_pd_data is a degrading parameter, then transform t_SU_MAR => t_pd_data_max. If t_pd_data is an improving parameter, then transform the -1*t_H_MAR => t_pd_data_min.

In case of timing graphs with existing propagation delays, increase/decrease any PCB trace by the above in the data path, or by the opposite for the reference path. If the two traces are on different types of layers, then they cannot be length matched; they have to be propagation delay matched. If a signal is partially routed on different layers, divide the t_pd for the two layers and calculate lengths separately.

For chips in bigger packages, like x86 chipsets or large FPGAs, the manufacturer provides "package length" information. This is a spreadsheet of routing lengths inside the package for every signal pin. For board design, the package lengths have to be included in the total length. For example, the Cadence Allegro PCB design software handles it as "pin delay."

Length constraints also can be signal quality-based, for example, to minimize crosstalk, reflections, stub-length and losses. The crosstalk noise voltage and the insertion loss are proportional to the trace length, and are normally simulated as per-unit-length PCB trace parameters. The SI-based rules are much less sensitive to the exact length than the t_pd based rules.

We can simulate two parallel traces at a unit length to get the crosstalk as an S-parameter in dB, then considering the maximum crosstalk-noise voltage we would permit, calculate a maximum parallel-segment length:

$$\text{length} \le \frac{V_{max} * \text{unitlength}}{V_{aggressor} * 10^{\frac{S_{unitlength}}{20}}}$$

Loss-based length constraints use the per-unit-length insertion loss at the signalling frequency:

$$\text{length} \le \frac{S_{max}}{S_{unitlength}} * \text{unitlength}$$

Longer PCB traces have stronger inter-symbol interference as well, which affects propagation delays through the transition time increase. Differential-pair phase tolerance skew slows down the differential slew rate, closing the eye from the corners. If skew exceeds rise time, then it closes the eye from the sides as well.

Typical PCB Design Rules

Usually the reference path and data path are handled separately. Specify maximum clock skew (in case of a central clock source), or just calculate min./max. data length based on the already routed clock length (if the clock is supplied by one of the chips). To have all the constraints in advance, then based on the floor plan, the clock length can be specified that is the shortest possible but still easily routable and then its value set as a tight absolute length range. Then, use t_pd_clk_min./max. as input parameters to the timing margin calculations. The amount of clock skew (in case of a central clock source) tolerable can be calculated from a pre-layout timing margin with zero skew, and permit 10% of that margin to be clock skew.

Usual PCB design rules:

- Min./max. data bus length.
- Min./max. clock trace length or max clock skew.

An asynchronous interface also has min./max. absolute length rules. The reference signal is always supplied by the master chip. The design rules are min./max. trace lengths for the data signals based on predefined strobe trace lengths.

Usual PCB design rules:

- Min./max. data bus length.
- Min./max. strobe trace length.

Source synchronous systems are designed in such a way to ensure the data and reference signal (strobe) paths have similar delays on-board and on-chip, except the DLL inserted into the reference path. This means the goal is to keep the data signal length within a +/-delta_length window around the strobe trace length. This is the simplest to design, since we are not restricted to using a predefined reference length.

Usual PCB design rules:

- Maximum strobe-to-data skew: as a relative length comparing to the strobe signal's length. As speed increases, both the min./max. delta length values get closer to zero. In a usual DDR3 memory interface, specify a maximum 0.125 mm delta length.

The usual design constraint is "matching with an offset." A simple explanatory equation can be derived from the generalized setup and hold equations:

The data t_pd has to be roughly between the clock t_pd and the clock t_pd plus the clock period.

$$t\_pd\_clk + other < t\_pd\_data < t\_pd\_clk - other + t\_clk$$

Calculate minimum and maximum length difference of the data signal trace length relative to the clock trace length. It will be asymmetric.

Usual PCB design rules:

- Maximum clock-to-data skew.
- Clock skew: If the clock generator is not inside the transmitter chip, then we have to balance the setup/hold margins with clock delay control.

Clock forwarding interfaces work in the same way as the unidirectional synchronous type, just that they support both read and write operations with separate clock signals for them.

Usual PCB design rules:

- Maximum clock-to-data skew, separately for read and write.

The only trace length rules are signal quality-based and lane-to-lane matching rules.

First calculate min./max. propagation delays for the data signals based on the table below, then calculate lengths. Finally,

apply some overdesign so after the layout has been designed, much greater-than-zero timing margins can be expected.

The source synchronous system timing can be handled in an absolute or in a relative way. The equations can be written in the same way as the synchronous systems, then the improving t_pd parameters changed to degrading parameters and multiplied by –1. After this, both the data and the reference t_pd will be degrading, sitting next to each other in the equations. Define delta_t_pd(+) = t_pd_data - t_pd_str, and replace the t_pd to these.

Steps for absolute rules:

1. Choose an absolute reference signal length (with a tolerance) or a maximum clock skew constraint.
2. Determine the reference signal t_pd from signal integrity simulation.
3. Determine the transition delay of the data signal using an estimated trace length.
4. Calculate all the timing margins, where the data signal t_pd is zero. Use t_pd_ref_min./max. as input parameters. If t_pd_clk is improving, then use minimum value, otherwise use maximum.
5. Convert the timing margins to min./max. t_pd for the data signals based on TABLE 2.
6. Calculate min./max. lengths for the data signals based on t_pd.

Steps for relative rules:

1. Calculate all timing margins, where the data signal and reference signal t_pd both are zero.
2. Transform the timing margins to min./max. t_pd for the data signals, relative to the ref. signal.
3. Determine the transition delays for both the data and the reference signal, based on estimated trace lengths.
4. Calculate min./max. delta_lengths for the data signals.

The length calculation. If the driver/receiver circuits of the data and reference signals are the same, then exclude the transition delay from the relative length calculation, since their transition delays will be near equal. This way their propagation delay matching is simplified to be trace length matching. If L_min > L_max or L_max < 0, then it is not possible to design a board at the given parameters.

Steps:

1. Get the transition delays at the receiver by a signal integrity simulation using estimated trace lengths, both minimum and maximum.
2. The propagation velocity (v) has to be calculated at the signalling frequency:

$$v = \frac{c}{\sqrt{\varepsilon_{r\_eff}}}$$

where c is the speed of light (3*10^8 meter/sec), Σ_{r_eff} is the effective dielectric constant of the materials surrounding the PCB trace.[4]

3. For absolute rules Length_min = v * (t_pd_min – transition_delay_min) and Length_max = v * (t_pd_max – transition_delay_max). For relative rules delta_Length(+) = v * (t_pd_max - transition_delay_data + transition_delay_ref) and delta_Length(-) = v * (t_pd_min - transition_delay_ref + transition_delay_data). Use min transition delay for maximum length, and maximum transition delay for minimum length, but only if the two signals are not driven by the same chip. Otherwise, both min. or both max.

The overdesign factor (OVDF). After calculating trace length constraints are ensuring minimum zero timing margins, make the system more robust by applying some overdesign. Here we introduce the Overdesign Factor (OVDF= {1.1…20}) for the tightening.

Length_range = Length_max – Length_min

Length_min_new = Length_min + 0.5 * Length_range * (1 - 1/OVDF)

Length_max_new = Length_max - 0.5 * Length_range * (1 - 1/OVDF)

Transforming and summing constraints is simple algebra, but it might not be straightforward. To transform a min./max. length rule to an Offset+/-Delta, use the simple formulae:

Offset = (length_min + length_max)/2

Delta = length_max – Offset

The second case calls for merging two constraints. For example, the chipset design guide provides direct trace length rules for interfacing a DIMM memory to the processor, and we want to design a memory-down layout based on JESD21C guidelines. In such cases, transform both constraints to Offset+/-Delta description, then sum the offsets and deltas separately.

Conclusions

High-speed digital board design requires control of the trace lengths pin-to-pin on multipoint signal nets. To achieve this, software supports detailed complex trace length constraints. Sometimes designers can use standard trace length rules specified by chip manufacturers or standards, while other times they calculate them from pre-layout timing analysis. If the board designer did not use proper length constraints, the boards may never even start up in the lab. Often, timing parameters for the chips on the board are needed, but just not available. In those cases, timing parameters defined at package-pins can be used. What the post-layout timing analysis reveals is not whether the prototype board will start in the lab, but if it will operate reliably in the field at all times. If this verification is absent in product development, the risk is untraceable errors in products will be detected by customers.

Ed.: For a list of references, see the online version at pcdandf.com.

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TABLE 2. Converting Timing Margins to t_pd Limits

INTERFACE TYPE	T_PD_MIN =	T_PD_MAX =	TYPE
Synchronous	- 1 * min(t_H_MAR_RD; t_H_MAR_WR)	min(t_SU_MAR_RD; t_SU_MAR_WR)	*
Asynchronous	- 1 * min(t_H_MAR_RD; t_H_MAR_WR)	min(t_SU_MAR_RD; t_SU_MAR_WR)	Absolute
Source synchronous	- 1 * min(t_H_MAR_RD; t_H_MAR_WR)	min(t_SU_MAR_RD; t_SU_MAR_WR)	Relative to strobe
Clock forwarding	- 1 * min(t_H_MAR_RD; t_H_MAR_WR)	min(t_SU_MAR_RD; t_SU_MAR_WR)	Relative to clock
Unidirectional synchronous	- 1 * t_H_MAR	t_SU_MAR	Relative to clock
Embedded.Clk	-	-	Lane-to-lane matching is relative
Arbitrary, timing graph	- 1 * t_H_MAR	t_SU_MAR	Relative to the original t_pd_data, if taken into account in the timing graph; otherwise absolute

HOT in the Valley

San Jose showed once again why it's the epicenter for printed circuit design. by MIKE BUETOW

The outside temperature hit 103°F in the Silicon Valley, but inside the action at the PCB West trade show was even hotter.

Attendance at PCB West in late September was up markedly – 26% for the exhibition and 35% for the conference. Overall attendee registration jumped 20.4%, as the industry responded with vigor to the strong lineup of exhibitors, complemented by an outstanding technical program.

Signal integrity remained a major area of interest, although during the PCB Designers Roundtable – cosponsored by the good folks from the Silicon Valley Designers Council chapter – it was revealed that perhaps one-third of designers don't actually perform SI analysis. (It's left for someone else.) Proponents on hand, including the ubiquitous Rick Hartley, who taught several classes during the three-day technical conference, stressed that all designers should perform some level of SI. Also revealed: A large percentage of designers continue to manually route their boards, despite evidence showing autorouters could save time. Whether they do so because they are trying to protect their jobs is certainly understandable, but the notion that autorouting could free up resources that could then be used in other areas (such as SI analysis) bears consideration.

Many of the technical sessions that accompanied the trade show were packed, as designers and process engineers took advantage of the free sessions to glean valuable information on reducing layer counts, thermal management, post-assembly cleaning, and CAD-CAM. In one eye-opening presentation, Don Trenholm of Custom Analytical Services literally ran out of time showing slides of various counterfeited components.

On the show floor, several companies either showed new tools and services or discussed pending upgrades.

National Instruments (ni.com) is releasing an upgrade to its MultiSim and Ultiboard suite for design optimization, schematic capture and SPICE simulation. The new release will include upgrades to handle power components, simulation improvements, IPC land patterns, more user-defined functionality, and stronger encryption. "We are starting to bridge the point where we can do a design, the virtual testing and then see how they compare," general manager Vince Accardi explains.

Be wise; use SI: Instructor Rick Hartley explains differential pair routing to an SRO crowd.

Flow through: Mentor sees opportunities in PCB thermal management.

Heavy flow: Show floor traffic was up 26% year-over-year.

Straight talk: AcAe technical director Clive Robinson pitches prospective customers on the firm's translators.

(For NI, the show also marked a changing of the guard of sorts, as Accardi and longtime product manager engineer Bavesh Mistry have been promoted, and former R&D engineer Natasha Baker is taking over the latter's role as PME.)

Mentor Graphics (mentor.com) touted its latest FloTherm thermal analysis tool, which helps designers identify thermal bottlenecks and shortcuts where new thermal paths would cool the design faster. The tool can perform a detailed simulation of the package itself, and users can overlay the component thermal model (which allows black box simulation) to simulate the package and complete PCB.

As long as there have been CAD tools, there have been translation problems. Not surprisingly, then, several companies showed various flavors of ECAD translators. SFM Technology's PackageWright (packagewright.com) tool combines an online database of thousands of package models with footprint generation capability and an ECAD-MCAD library synchronization service. The tool supports flow from MCAD-ECAD and back.

AcAe (acae.com) drew a crowd with its DART ECAD conversion tool. Noting that the EDIF schematic and netlist translator format was launched more than 25 years ago, AcAe president Bill Basten said the biggest problem designers and manufacturers now face is that many translators simply don't work. "The schematics don't match; they can't do constraints; they leave things out." DART, he says, which runs on Linux and Windows, verifies netlists and copper, and permits use of libraries and symbols, provided they are similar.

A large number of DESIGNERS CONTINUE to manually route PCBs.

PCB West has an emerging assembly bent to it, highlighted by several tracks on counterfeit component identification and mitigation, post-assembly cleaning and test strategies. Classes on thermal management and layer reduction were also popular.

By providing PCB engineers, designers, fabricators, assemblers and managers with the most targeted conference in the industry, PCB West proved the market for board-level shows isn't dead after all. Full details regarding the conference and exhibition are available at pcbwest.com.

Following this year's successful show, PCB West will return to the Santa Clara (CA) Convention Center Sept. 27-29, 2011. PCD&F

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PCB Thermal Design DEVELOPMENTS

New 3D thermal quantities help designers address thermal problems as they arise. by BYRON BLACKMORE, JOHN PARRY AND ROBIN BORNOFF

Electronics thermal management is the discipline of designing electronics systems to facilitate the effective removal of heat from the active surface of integrated circuits to a colder ambient environment. In doing so, heat passes from the package both directly to the surrounding air and via the PCB on which the IC is mounted. The PCB and, to a lesser extent, the surrounding air thermally couple the various heat sources.

Heat coupling increases as components and PCBs become smaller and more powerful. Designers must take remedial action to bring all components within their respective thermal specifications, but this step is becoming more challenging and constrained, even when preventative measures are taken early in the design process.

For the past 20 years, computational fluid dynamics (CFD) techniques have provided 3D thermal simulations that include views of the air-side heat transfer that predict component junction and case temperatures under actual operating conditions. Designers routinely use these predicted temperatures to judge thermal compliance simply by comparing the simulated temperatures to maximum rated operating temperatures. If the operating temperature exceeds the maximum rated value, there will be at least a potential degradation in the performance of the packaged IC, and at worst, an unacceptable risk of thermo-mechanical failure.

Simulated 3D temperature and flow fields provide detailed and useful information, but give little physical insight into why the temperature field is the way it is. Examining heat flux vectors can yield some insight into the heat removal paths. But the heat flux vector direction and magnitude data do not provide a measure of the ease with which heat leaves the system. Nor do they provide insight as to where and how the heat flux distribution might be better balanced or reconfigured to improve performance.

How easily heat passes from the various sources to the ambient will determine the temperature rise at the sources and all points in between. Heat flow paths are complex and three-dimensional, carrying portions of the heat with varying degrees of ease. Paths that carry a lot of heat but offer large resistances to that heat flow represent bottlenecks. A redesign can relieve these bottlenecks, permitting heat to pass to the ambient more easily and reducing temperature rises along the heat flow path all the way back to the heat source. In addition, there may be unrealized opportunities to introduce new heat flow paths that would permit heat to pass to colder areas and out to the ambient. So a redesign informed by the right information can do more than alleviate bottlenecks; it can also introduce thermal "shortcuts" to bypass them.

Sans a way to identify such thermal bottlenecks and shortcut opportunities within a design, PCB design teams have faced a stark choice. Either bring in thermal experts to resolve thermal problems, or rely on being able to add heat sinks later. Lacking direction from the simulation results as to appropriate remedial action, thermal engineers have traditionally relied on experience and engineering judgment to guide their search for design improvements. Today their work is often supplemented by design of experiments and automatic design optimization capabilities within the thermal simulator. Such approaches take time.

An innovative way to view the thermal behavior of a populated PCB uses two new 3D thermal quantities aptly known as the BottleNeck (Bn) Number and the ShortCut (Sc) Number that, taken together, guide designers to take appropriate, targeted remedial action to address thermal problems as they are encountered.

Vectors, Bottlenecks and Shortcuts

Heat flow can be defined in terms of a heat flow through a given cross-sectional area. This measure is known as a heat flux. The presence of a heat flux vector will always be accompanied by a temperature gradient vector. The temperature gradient field is taken to be an indicator of conductive thermal resistance as, for a given heat flux, the greater the temperature gradient is, the larger the thermal resistance will be.

The dimensionalized Bn number is the dot product of these two vector quantities. At each point in space (**FIGURE 1**) where there exists a heat flux vector and temperature

gradient vector, the Bn scalar at that point is calculated as:

Bn = Heat flux magnitude × Temperature gradient magnitude × sting bottlenecks.

This is not always true, of course, especially for multiple heat sources (as found on almost every PCB) where heat flow topologies for widely separated components can be quite independent of each other.

To illustrate how this process works in practice, consider a typical air-cooled PCB (**FIGURE 2**). The central BGA has highest temperature rise above specification, followed by the two TO-263s above and to the right.

Though it depicts the same PCB, **FIGURE 3** is not the same kind of thermal view as Figure 2. Instead, it shows the Sc number distribution mapped at a point just above the tops of the packages on the board. Although in Figure 3 the largest Sc numbers are associated with the hottest component, this is not always the case. A component might be hot due to the temperature of the surrounding air, rather than its own internal power dissipation. In the case of this centrally located BGA, the large Sc values on its top surface indicate relatively efficient convective heat transfer locally. Therefore, the obvious remedial design action is to add a heat sink. The heat sink acts as an area extender, making it even easier for heat to leave the top of the component and to be carried away by the air. Introducing this design change reduces the BGA's junction temperature rise by 70%, taking it well below its maximum safe operating limit. With the BGA running thermally compliant, let's turn our attention to the TO-263 components.

FIGURE 4 is a Bn plot depicting the Bn distribution in the top signal layer of the PCB. We can see that, after adding the BGA heat sink, the largest thermal bottlenecks exist near the tabs of the two TO-263 devices. Recall that large Bn values do not mean this is the hottest area. Instead, the Bn figures and the plot reveal areas in which a lot of heat flows "downstream" from the heat source, and is highly restricted. Knowing exactly where the bottleneck is, a large copper pad can be added to cover that high bottleneck area, providing a targeted solution to a specifically identified problem. That is effective, efficient engineering.

Having made this modification,

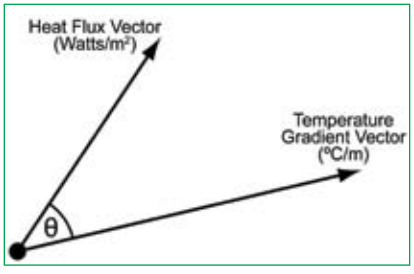

FIGURE 1. Misaligned heat flux and temperature gradient vectors.

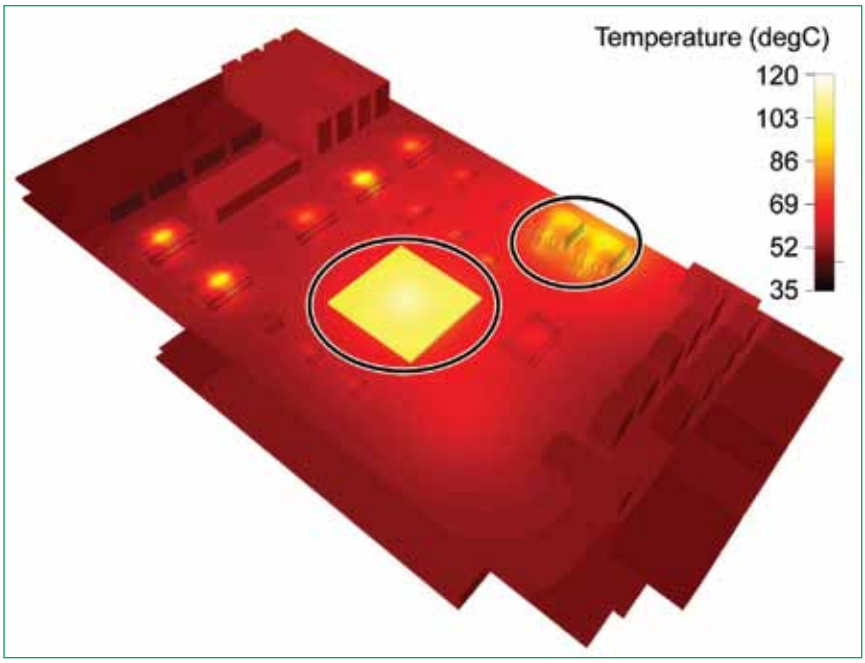

FIGURE 2. PCB temperature distribution as predicted by CFD analysis. Circles indicate the hottest components on this board.

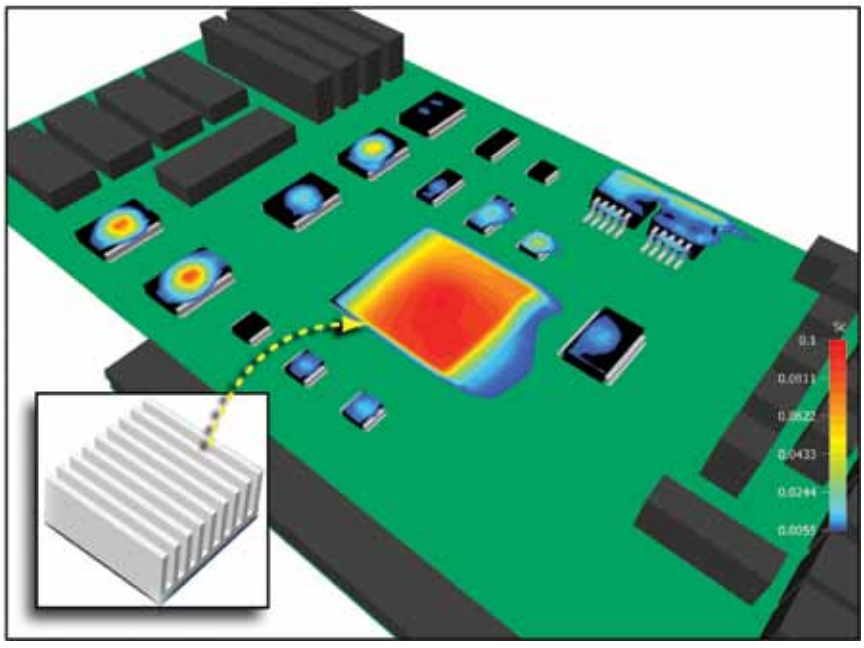

FIGURE 3. Sc Number distribution above package tops. The colors on the BGA device indicate a relatively efficient convective heat transfer locally, which offers an opportunity to reduce the temperature increase by adding a heat sink as shown.

best practice methods call for an updated thermal simulation and inspection of the new Bn and Sc distributions. **FIGURE 5** shows Sc on a cross-section through one of the two TO-263s after the addition of the copper pad. The expanded inset view shows large Sc values on the signal layer and the power and ground planes below the new copper pad and TO-263 tabs, indicating a shortcut opportunity between these layers. This agrees with a designer's intuition, since heat spreads readily in the metallic layers of the PCB, while the dielectric's low thermal conductivity acts as an effective barrier to heat transfer. Adding thermal vias to create a new heat transfer path down to the buried ground plane is an excellent, practical way to take advantage of this shortcut opportunity. Note that the Sc field pinpoints exactly where the thermal vias should be added for maximum effect.

By examining the Bn and Sc variations in and around the TO-263, the exact shape of the copper pad and the location of an array of thermal vias (shown schematically in **FIGURE 6**) can be determined quickly, without resorting to numerous "what if" studies. In this case, adding the pad and vias yielded a 30% drop in the temperature rise of the TO-263 devices, again taking them below their maximum rated temperatures.

The Bn and Sc fields together provide invaluable insight and comprehension about temperature distribution and behavior in an electronics system. By detecting and mapping both thermal constrictions (bottlenecks) and potential shortcuts for more efficient heat transfer, these parameters enable engineers to quickly determine the most promising thermal design changes – those most likely to provide the most efficient, effective results – without years of thermal experience and intuition.

In the example, three Bn- and Sc-inspired thermal design changes were identified quickly, and the resulting "fixes" dramatically reduced the temperature of the three overheating components discovered in the initial simulation. It is an approach that delivers important gains in simulation productivity. Rather than simulating all possible remedial actions for thermal problems and choosing the best one, engineers can see immediately where they need to focus their thermal design effort. PCD&F

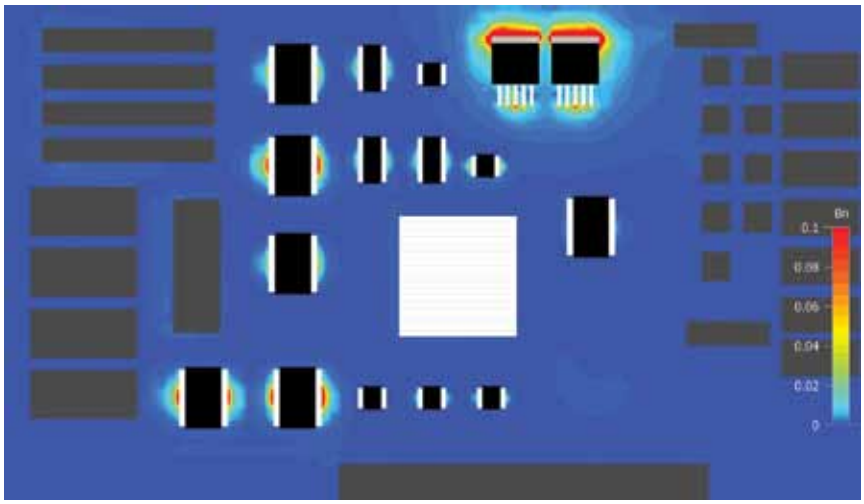

FIGURE 4. Bn Number distribution on top signal layer.

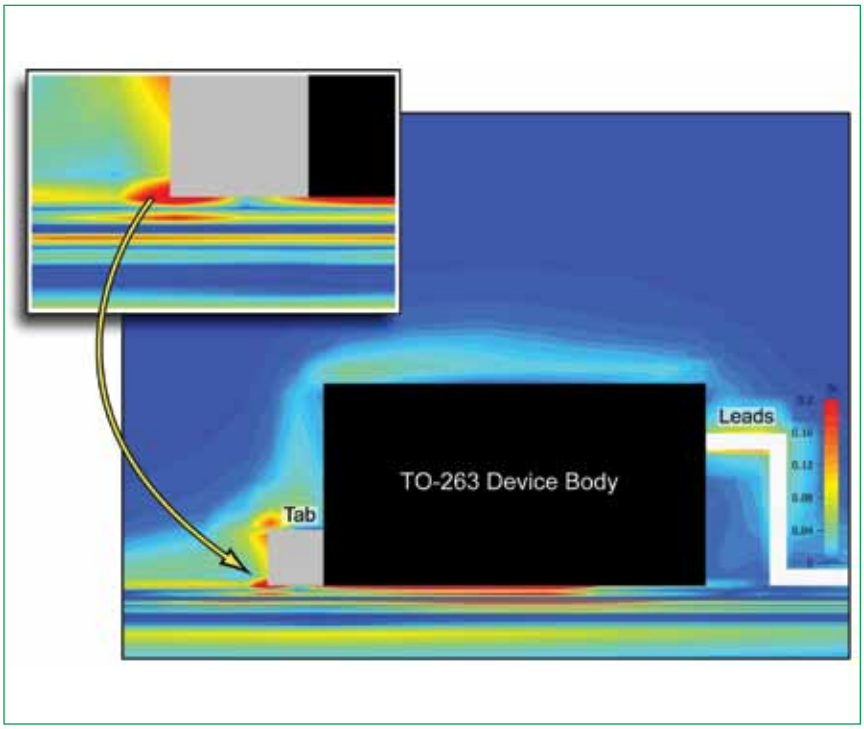

FIGURE 5. Sc Number distribution through TO-263.

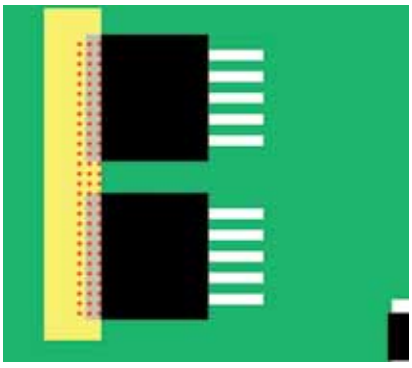

FIGURE 6. Addition of copper pad and thermal vias.

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MSD PROTECTION STEPS Per J-STD-033B.1

Procedures for preventing and ridding moisture from components.

by DON SHELL

As packages get smaller, the risk for damage to moisture-sensitive devices increases. With the higher temperatures required for Pb-free soldering, that risk is further compounded.[1] That's why it's extremely important to be aware and vigilant of MSDs.

ICs can act like a sponge. If they have semi-permeable membranes, moisture from the ambient air can get into those devices. When they get rapidly heated during reflow or rework, the result is rapid outgassing. In some cases, this excessive outgassing causes popcorning, which can damage the internal structures of a component.[2]

To minimize and eliminate the adverse effects related to MSD, assembly personnel, process engineers and technicians must diligently apply regimented practices based on the IPC/JEDEC J-STD-033B.1 standard. This standard sets out a long list of procedures that must be implemented for handling, packaging, and shipping MSDs.[3]

Protecting and controlling MSDs on the assembly floor takes into account a great number of large and small procedures and important steps. Violating, ignoring or overlooking any or a series of these precautions could result either in costly rework or latent PCB defects.

More often than not, electrical test catches the popcorning problem in an MSD. But in this instance, damage may not immediately lead to a failure and instead present itself as a latent defect. Subsequently, such a component compromises a finished PCB and can lead to system failure in the field. Therefore, trained process engineering personnel, experience, and a highly disciplined and structured assembly operation are critical to protect surface mount components from humidity present in an assembly environment.

Affected components can include any surface mount devices, ICs and discrete devices that mount to one surface of a PCB when assembled.[3] MSD components are specified by their respective manufacturers to have a limited floor life at or below 30°C or 86°F and 60% relative humidity (RH).[3]

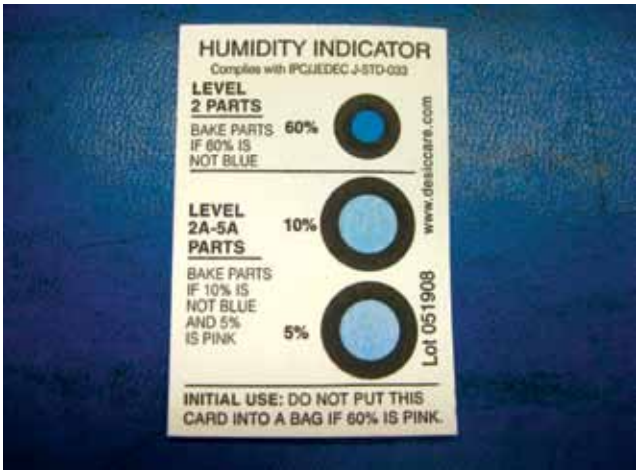

FIGURE 1. Humidity indicator card with moisture-sensitive chemical dots.

Tools of the Trade

Four materials and techniques help protect and control MSDs. Those are moisture barrier bags (MBB), desiccant, humidity indicator cards (HIC), and moisture-sensitive caution labels. Storing MSDs in MBBs provides the first line of protection and restricts transmission of water vapor. Desiccants further boost MSD control when used to absorb moisture that gets into the MBB or is sealed in it. It's also advisable to include more desiccant to absorb moisture in component carrier materials such as trays, tubes and reels.

The HIC does its part with its moisture-sensitive chemical dots (**FIGURE 1**). Those dots change color from blue to pink when indicated RH is exceeded inside the MBB. The card must have a 5, 10, and 60% RH sensitive dot. The HIC has instructions for when to bake parts, depending on the moisture sensitivity level (MSL) of a particular device. For example, if a device has an MSL of 2, then the parts need to be baked if the 60% dot is not blue.[3] For devices of MSL level 2A-5A, then parts need to be baked if the 10% dot is not blue and the 5% dot is pink.[3]

MSL is the classification of the MSD's floor life for the Pb-free condition or SnPb soldering condition at the factory ambient environment (≤30°C/60% RH). The MSL for Pb-free processes is higher than the MSD for SnPb process

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FIGURE 2. Technician vacuum seals moisture-sensitive devices.

for the same component. The higher MSL has a shorter floor life than the lower MSL. Floor life means the out-of-bag life, not including the life in the safe storage. Therefore, for the specific reflow process, the proper MSL must be chosen. Misusing SnPb MSL for the Pb-free reflow process results in MSD damage from moisture absorption and yield/reliability degradation that can affect products in the field.

Most moisture-sensitive components are MSL 3 for SnPb soldering and MSL 4 for Pb-free soldering. For example, a moisture-sensitive BGA component has two MSL markings on its MS label: MSL 3 for SnPb process and MSL 4 for Pb-free process. This means that it has 168 hr. of exposure time to factory ambient environment if used in SnPb reflow, or 72 hr. of exposure time if used in Pb-free reflow.[3] Compared to the traditional SnPb reflow process, its Pb-free process air exposure time is reduced 57%. Special attention must be paid to tight floor life management for RoHS projects.

Some MSD packages have multiple MSL markings: 2/240 and 3/260. This means that for SnPb reflow (peak temperature of 240°C), an MSD can be treated as level 2 MSD. For Pb-free reflow (peak temperature of 260°C), this MSD should be treated as level 3 MSD with shorter air exposed time (floor life).

At the outset, it is the responsibility of the assembler to require all suppliers and customers to follow J-STD-033B.1. The assembler must be sufficiently vigilant of suppliers' and even customers' poorly packaged and shipped MSDs that violate the standard. It's also the assembler's duty to keep suppliers and customers accountable for maintaining procedures in accordance with J-STD-033B.1.

An assembler's receiving and stockroom has its own agenda for controlling MSDs, as well as strictly following J-STD-033B.1. Foremost is creating and maintaining an MSD control event logbook to record specific problems and solutions on given dates, and verify such information with an inspector's signature. Incoming QC inspectors check whether the 5% dot is pink. These personnel should also inspect and, when necessary, reject damaged dry pack components, unsealed dry packs, missing desiccant or HIC dry packs. An operator must copy the MS level and floor life to new MBB labels when transferring MSD components to a new MBB.

From a general MSD environmental control perspective, the assembler must install digital temperature and RH meters in the stockroom and SMT production areas. MSD handlers read in real time data involving floor temperature, floor RH and the out-of-bag total time during the assembly process, and out-of-MBB environment. Based on that data, they implement MSD procedures and record MSD condition information. Meanwhile, production managers monitor factory ambient conditions. If room temperature exceeds 30°C (86°F) or room RH is more than 60%, floor life indicated on the MS label is no longer applicable and must be de-rated.

In keeping with the standard, it's also important to be well stocked with certain items. Those include foam covers or bubble wrap for use around a stake of trays inside the MBB to avoid puncture during the sealing process. ESD-safe black card paper must be used to cover a tray's bottom and top sides before it is inserted into an MBB. Moisture barrier bags and a vacuum-operated bag-sealing machine are vital as well (**FIGURE 2**). Special care must go toward using this machine, and the vacuum must be sufficiently relaxed to keep the tube or tray from puncturing the bag.

Baking Procedures

MSD control at the kitting stage involves three major steps. First, process engineering personnel must separate large quantities of MSD packages into small quantities based on the running batch size. Next, certain procedures are performed to properly receive all production-returned MSDs. All returned MSDs are to be resealed. Personnel ensure MBBs are identified with correct part number, quantity and MSD label. Last, manufacturing personnel properly arrange bake time to meet production requirements.

Another trio of steps is involved for production scheduling. First, for water-soluble-paste double-sided MSD boards, technicians finish both sides on the same day without washing between bottom and top reflow. Second, on the same day, they must finish all rework before sending the jobs to washing. One or two days before production, technicians arrange incoming QC of all MSDs. At the same time, they ensure there is sufficient time to bake those MSDs, keeping in mind that some MSD BGAs require 48-hr. baking. Third, technicians track MSD floor life and exposed time, as well as monitoring any noncompliant issues.

Meanwhile, in the SMT area, an SMT operator should record bag-open-

ing date and time, as well as check and report to the floor manager any MSDs with longer floor life than that marked on the bag. Another procedure is to have SMT or other production and engineering groups return all remaining MSDs when their jobs are completed. Following that procedure, stockroom technicians re-seal all MSDs and record sealing data and time.

In some cases, assemblers will find it necessary at the kitting stage to bake MSDs before placing them on the production floor. If shelf life or RH on the HIC has been exceeded, components need to be baked until the moisture is removed. There are at least a half-dozen steps that must be carefully performed to bake components according to spec.

For example, it must be understood that baking degrades MSD solderability, thus causing quality problems.[2] To avoid degrading solderability, a cumulative bake time limit of 48 hours at 125°C is imposed.[3] However, floor personnel must be alert to the fact that MSD baking conditions depend on component body thickness and MS level.

Further, they are not to bake mixed MSDs with different body thicknesses in the same baking oven at the same time. Another similar procedure is "don't bake mixed MSDs with different bake time at the same time in the same oven." It is also a good practice to have separate baking ovens for PCBs and components and a detailed log maintaining all the records.

Each MSD can be baked only one time, and no second baking is allowed. Moreover, an MSD without clear MS Level marking on the package is not to be baked. Baking temperature is 125°C for 24 hr. with tolerance range for temperature control ±5°C (120–130°C). Baking time should follow IPC J-STD-33B.1, Table 4-1.

Different MSD component trays/carriers have different maximum bake temperatures. It is vital always to check the tray bake temperature for each tray before sending it into the bake oven. Also, floor personnel should collect, recycle and store 140°C or higher MSD trays with different sizes. Use them to replace the low bake temperature trays from suppliers or customers. A final procedure for any assembler to follow is if floor personnel don't know the MSD baking history, it is time to stop MSD baking. CA

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3. IPC/JEDEC J-STD-033B.1 - Includes Amendment 1, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, January 2007.

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CIRCUITS ASSEMBLY

Conformal Coating Coverage

Low solids coatings may lead to poor coverage.

THIS MONTH WE feature a conformal coating issue. Does it meet standards, or is it a reliability concern?

Conformal coating sharp corners can be difficult. The flat surfaces on this PLCC device (FIGURE 1) show satisfactory coating and, provided the surface of the board and all terminations and separation gaps between adjacent exposed pads are covered, the reliability of the product should be satisfactory.

Based on many standards, however, the non-coverage or edges of plastic parts would be considered unacceptable. It is felt that inspection. It could be argued that if the coating were to fail in these areas, it could peel off the rest of the board.

To achieve a better coverage on devices like this, it would be necessary to coat the board assembly again, but also consider the viscosity of the material used. If the solids content was low, it may have reduced coating coverage. This type of process issue is more likely to be seen on spray rather than dip coating and is exaggerated on plastic components if cleaning is not part of a standard process.

These are typical defects shown in the National Physical Laboratory's interactive assembly and soldering defects database. The database (http://defectsdatabase.npl.co.uk), available to all this publication's readers, allows engineers to search and view countless defects and solutions, or to submit defects online. CA

FIGURE 1. This PLCC would pass conformal coating standards for coverage, but a second coating would ensure gaps are filled.

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Avoid the BGA Voids

Cross-sectional analysis may be the tool to assess failures.

MOISTURE DAMAGE USUALLY appears as physical damage to the component. The first indication would be externally observable changes to the package in the form of bulging or fractures to the outer surface of the component. Internally observable indicators of moisture damage typically include fractures to the die inside the package and lifted or fractured wire bonds. These conditions would be apparent during transmissive x-ray inspection. Another symptom of moisture would be inconsistent solder joint sizes that result from package deformation during the liquidus phase of the reflow process. No issues were observed with the large BGA components here (FIGURE 1). X-ray showed that the die, wire bonds and solder balls appeared well-formed and provided no indication as to a loss of functionality.

For smaller BGA style components, however, assembly and solder workmanship issues were identified (FIGURE 2). Specifically, the elevated level of voiding in the solder joints on the 54-pin memory components was identified as a potential contributor to failures. IPC-A-610E specifies voiding that exceeds 25% of the x-ray image area is a defect for all classes of production. We recommend that any voiding that exceeds 10% of the ball x-ray image area be treated as a process indicator (i.e., a condition that indicates excessive variation from the intended result). Although detailed voiding analysis was not performed on these samples, it was apparent from visual inspection there were many solder joints on these parts that exceeded the 10% recommended limit. Many voids appeared to be at an interface, which may have contributed to signal issues. The sizes of the voids also may have interfered with long-term reliability.

The location of voids in a BGA solder joint can be critical, regardless of the void size. Voids that occur at the solder joint/PCB land interface ("interface voids") can impact the reliability of the resulting solder joints. This occurs because solder joint yield strength is related to the surface area of contact between the solder and the surfaces it joins. Interface voids reduce this contact area and can lead to mechanical failure of the solder joint. Some solder joints, such as those in Figure 2, appeared to have voids that occurred at the interface and have reduced the wetting contact areas on the PCB.

Voiding has a variety of causes, including the properties of the flux and the reflow profile. Interface voids can also be a result of a non-wetting or dewetting condition on the PCB land. No other assembly workmanship issues were detected during inspection. Voiding that occurred on components other than the 54-pin memory was minor in nature and fell within the expected amount of voiding on a well-formed BGA solder joint. All solder joints (except those noted) showed evidence of good collapse and wetting to the PCB lands, as would be expected on a well-formed BGA solder joint.

We recommended further investigation of the voiding observed on the 54-pin memory components, specifically 1) the process used to assemble and solder the memory components, and 2) the interface voids. The interface voids should be investigated to determine if their location actually is on the interface. Cross-sectional analysis could be used to specifically examine a solder joint of interest and accurately determine the location of the void. This analysis would include evaluation of the PCB land for evidence of any contamination or metallurgical issues that would result in improper solder wetting.

The voiding level observed on the 54-pin memory should be reduced by adjusting the assembly process. One method is to test alternative solder pastes. Another is to adjust the reflow profile. Both methods can be used together, or modifications to the reflow profile can be performed using the existing paste. We also recommend cross-sectional analysis of the samples and x-ray analysis of future samples produced on a modified reflow process. CA

ACI TECHNOLOGIES INC. (aciusa.org) is the National Center of Excellence in Electronics Manufacturing, specializing in manufacturing services, IPC standards and manufacturing training, failure analysis and other analytical services. This column appears monthly.

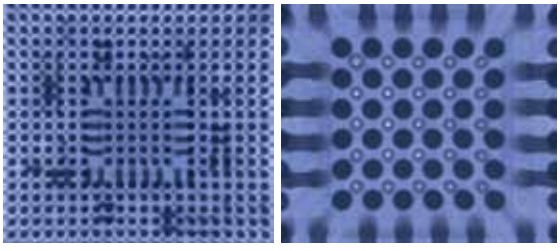

FIGURE 1. X-ray of BGA component shows minimal voiding (left) and intact wire bonds (right).

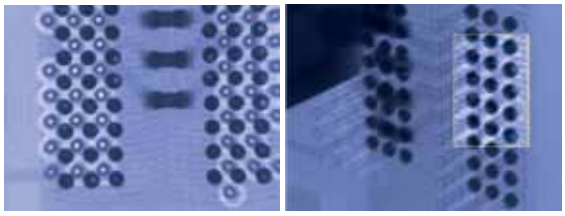

FIGURE 2. A smaller BGA showed significant solder ball voiding (left). An oblique angle view (right) shows voiding on the solder ball edges.

How Low Can You Go?

Lower-concentration cleaning agents are one response to "green" demands.

WRITING THIS COLUMN is a tremendous opportunity to comment on the rapidly changing world of precision cleaning within electronics. In short, cleaning is becoming more difficult and more demanding. It is our job to meet these new challenges head on and translate them into opportunities. So, what is changing, you might ask?

For one, the increasing local and global (i.e., RoHS, UNEP, GHS, etc.) initiatives to become "greener" have customers requesting more environmentally sound process solutions. At the same time, the need to clean better under low-standoff components has arisen. And, if that is not enough, customers expect more engineering support to identify additional improvements to their cleaning process, leading to a lower cost per cleaned part.

While we all understand and embrace efforts to provide our children with a safer and healthier world, we cannot easily ignore the effects of the global recession. At first glance, it seems that this calls for some tough choices. How can we continue to produce high-reliability products on a tighter budget, while implementing new and green technologies? Often, innovations as well as cost savings require upfront investment. It is here where we have to educate our customers about the solutions they might not be even aware of.

Let's take a few prime examples to illustrate the possibilities of making a cleaning process greener:

- Lower, yet stable, operating concentrations to minimize chemistry consumption.
- Elimination or reduction of volatile organic compounds (VOC).
- Cleaning agents with lower pH levels to reduce effluent operating costs.

Operating chemistry concentrations is one topic I have addressed in various previous columns. Greener cleaning processes can be achieved through lower and more stable concentrations that in turn help minimize chemistry consumption. One obvious fact: The higher the concentration, the higher the user cost. Factors such as the bath life of the cleaning agent also have to be taken into account. Assuming the same bath life, a lower concentration leads to direct savings, which is exactly what the latest cleaning agent technologies provide, as they can be used at 10% or less. It is also important to point out, however, that actual and perceived concentration can be two entirely different values. Once the operator begins to use the cleaning agent, the dissolved contamination affects the concentration measurement. Thus, overconcentration through ineffective measuring techniques can cost you handsomely. New bath analyzing technologies have emerged to help users accurately maintain concentrations. So, please, check your process, as this could lead to significant savings.

Second, VOCs are integral parts of many cleaning agents and serve a very important purpose. They support the cleaning agent's job by solubilizing organic contamination. Reducing VOCs generated by cleaning processes, however, is a worthwhile thought because it would minimize their environmental effects. However, if one were to simply eliminate VOCs from the cleaning agent, it would have detrimental effects on the cleaning results, and product reliability would be everyone's buzzword. On the other hand, numerous avenues do exist to control the environmental impact of cleaning agents containing VOCs. Most notable are vapor recovery techniques with efficiency rates between 15% and 85%.

Overconcentration through INEFFECTIVE MEASURING TECHNIQUES can cost you handsomely.

This type of investment in process improvements also can help minimize cost. Appropriate vapor recovery techniques such as "condensation" (through active cooling) not only help maximize the collection of chemistry, but also recover DI water. Both are subsequently returned to the wash tank and recycled in the process, leading to substantial cost savings and a minimal impact on the environment.

Third, pH-neutral products for defluxing and stencil cleaning have emerged and are undergoing test and implementation. Similar to vapor recovery, the use of pH-neutral products enables users to benefit from more environmentally sound process solutions at an overall lower price. Users can now directly dispose effluent water from the chemical isolation section (sometimes 5 gal./min.) without extensive wastewater treatment. Given an acceptable cleaning performance, these new innovations combine environmental benefits with process savings: a win-win situation for vendor and customer.

We should set goals for ourselves to work toward. Accepting the status quo or waiting for someone else to innovate does not exemplify leadership, nor does it show responsibility for tomorrow's world. So, how low can you go? CA

ED.: Those concerned about environmental regulations should read Kal Kawar each week at circuitsassembly.com/blog.

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芯片粘接技术的创新为叠层芯片应用提供了薄膜材料的替代方案

白洁 汉高公司

尽管在本专栏中我通常会关注主流的SMT材料应用，但我已经决定要更进一步转向上游应用环节，来谈谈一个在我看来相当令人兴奋的半导体封装工艺的新发展。装配商们对更小，更快，更便宜的范例并不陌生，这也正是本期专栏将要讨论的一个与器件制造相关的例子。

对于封装专家而言，这种小体积+强大功能的组合意味着需要加工更薄的晶圆和堆叠更薄的芯片。这里面有什么难题呢？那就是所有这一切都必须在低成本的前提下完成，这样才会让精明的消费者感兴趣并可能购买。

毫无疑问，就高度微型化器件的繁荣而言，芯片粘接材料技术的进步一直至关重要。尽管传统的芯片粘接剂和新的芯片粘接薄膜可解决某些应用中的诸多挑战，但它们存在弊端，并已经促成了叠层封装的一个创新解决方案：晶圆背面涂覆技术（WBC）。

人们普遍认为WBC材料与传统的芯片粘接剂相比有生产能力更高的优势，并且它们比薄膜材料成本更低。在过去的几年里，WBC材料已经被成功地应用在引线框架封装中。传统膏体状材料的涂覆是靠材料从注射器顶压挤出，是一系列过程，因此会限制生产能力。此外，胶层厚度的控制也与放置芯片的力密切相关，有可能会导致的情况包括胶层覆盖不足（力太小），胶层溢出（力太大）或芯片倾斜（力不均匀）。对于现今的超薄晶圆，大部分市场已转向使用芯片粘接薄膜，这是因为它们不仅易于操作，而且胶层覆盖薄且均匀。但是，与膏体材料一样，薄膜粘接材料也存在一些缺点，且并不仅仅局限于它们比膏体材料成本更高。为引线框架封装开发的WBC材料可通过丝网印刷，钢板印刷或旋转涂布的工艺来实现应用，与点胶工艺相比它大大提高了生产能力，并提供了一个替代薄膜材料的低成本解决方案。

虽然WBC材料在引线框架应用上很成功，但它们在历史上一直不被看作是一个可行的堆叠新式超薄晶圆的方法。这里面有几个原因：首先，在>75微米厚的晶圆上非常适用的高生产能力的涂布方法，如丝网印刷和钢板印刷，它们可能无法应用在今天的超薄晶圆上。其次，丝网留下的痕迹和通常由于刮刀横动所引起的“挖舀”效应有可能造成超薄涂层的厚度不均匀。其他替代方案，如旋转涂布，常会导致超过70%的材料浪费，这就抵消了WBC相对于薄膜所节约的材料生产成本。

然而，稳定可靠的材料配方与喷雾涂层技术的新发展相结合，从而提供了一个新的WBC解决方案，此方案能够克服叠层芯片应用中与薄膜和传统膏体材料相关的许多问题。新材料的配方能够满足多芯片叠层应用的要求，可用于如TSOP、MCP和FMC（闪存卡）封装的内存市场。

此项新WBC技术是为在线工艺处理而设计的一个解决方案，它对叠层芯片技术目前所基于的薄膜材料提出了一个强劲、可靠且成本低廉的替代方案。事实上，初步分析结果表明，新一代WBC材料可将用户总成本降低30%至50%。工艺灵活性也得到提高，这是因为封装专家们现在可以根据特定的生产要求来调整芯片粘接胶层厚度，也可以自主选择晶圆划片胶膜。而薄膜粘接材料在供应时通常其厚度已定，并与划片胶膜一起作为捆绑产品销售。

新的WBC工艺相当简单易用，它提供了一个在线处理的解决方案。在晶圆薄化过程之后，通过喷雾涂布的方法将WBC材料精确地喷镀在晶圆背面，然后进行紫外线照射处理得到B-阶材料。完成此步骤后，取下正面的研磨胶膜，然后将划片胶膜碾压粘贴到晶圆背面，再将晶圆划片好，以备芯片拾取和放置。

使用该方法也可为50微米厚的超薄晶圆加工涂层。目前正在进行的研发工作是为了实现制出5微米厚的WBC涂层，配方专家们预期在未来的12个月内将可实现此项应用。

敬请继续关注！

致谢：作者感谢汉高公司于媛媛和薛扬的宝贵意见。

FIGURE 1. 厚度为50微米、直径为200毫米的晶圆上涂有一层10微米厚的新一代WBC材料

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On the Forefront, continued from p. 18

Module Board (IMB), which embeds active and passive die in laminate structures, has been extended to flex circuits. A number of companies have developed processes incorporating resistors in flex circuit material, including Asahi Chemical Research Laboratory, DuPont, Ohmega Technologies, Ticer Technologies, and Endicott Interconnect. Buried capacitors in flex are offered by Oak-Mitsui Technologies, 3M Electronics, DuPont and Hitachi Chemical.

The flexibility of flex circuits will enable it to find applications in a variety of future products. New and exciting possibilities are expected of a technology that has been around a long time. **CA**

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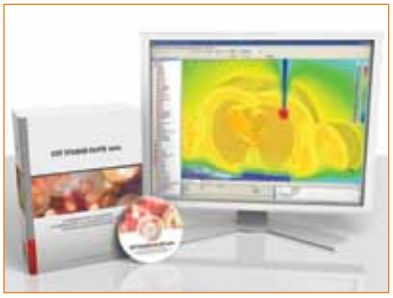
1. G. Kunkel, “Ultra-flexible and Ultra-thin Embedded Medical Devices on Large Area Panels, “ European Semantic Technology Conference, September 2010.



HIGH-FREQUENCY SIMULATION

CST Studio Suite 2011, including CST Microwave Studio, is for electromagnetic problems. Material property descriptions have been enhanced across available solvers. High-performance computing options are available for frequency domain and integral equation solvers. Time and frequency domain can provide sensitivity information for an arbitrary number of parameters in one simulation run.

Computer Simulation Technology
cst.com

INSPECTION KIT

Mighty Scope Pro Pack kit comes with two handheld digital microscopes and a polarizer attachment for electronics inspection, analysis and measurement. Includes scopes with 10x to 200x, and 500x magnification; polarizer for contrast-enhancement; accessories for hands-free operation; 1.3 Mp camera with 1/3" color CMOS image sensor; ergonomic design.

Aven
aveninc.com

CAD TOOL WITH AUTOMATED BOM

PCB123 v4 advanced software design tool has an intuitive CAD interface for freedom and flexibility in schematic and layout editing. Features 500,000 new parts, improved search functionality with complete access to parts libraries, automated BoM, and data importer that imports DXF files from mechanical CAD tools. Integrates DRC/DfM rules into the software. Offers research, availability and pricing for each component registered in the Digi-Key database. Is free and requires no license.

Sunstone Circuits
sunstone.com

OTHERS OF NOTE

LASER-DIRECT STRUCTURING

Fusion3D laser has upgraded optics and laser control. Reportedly cuts structuring times for 3D circuit boards 10% to 20%, depending on component layout. Includes improved laser head.

LPKF Laser & Electronics AG
lpkfusa.com

ECAD-3D TRANSLATOR

ACE Translator 3000 v.6 provides over 100 translators between most common EDA, CAD, and 3D formats, all in a single intuitive environment. Is said to simplify translation process. Built-in viewer is user-friendly with powerful editing and repair features. Outputted files optimized for compatibility with all design systems. Supports AutoCAD 2010 and AutoCAD 2011 DWG/DXF files. Export (Gerber, DXF, ODB++) will automatically detect Arcs. Can flash all selected objects at once to a chosen shape.

Numerical Innovations
numericalinnovations.com

LOW-PROFILE CONNECTOR

Space-Saver BNC connector mounts on the edge of a PCB. Is low profile. Reduces twisting stress on solder joints inherent in BNC connector mating. A notch in the connector slips over PCB edge prior to soldering, forming a tight mechanical fit that transfers majority of rotational energy to the PCB instead of solder joints. Has 75 Ω impedance and is tested to 2 Ghz.

Regal Electronics
regalusa.com

MSDS SOFTWARE

Online MSDS Management Solution manages system independently and bulk uploads hundreds of documents in minutes from anywhere in a secure environment. A hosted service, requiring no special software installation, new hardware or IT resources. Archives obsolete MSDSs for 30 years. Displays search results in real time. Tracks inventory, VOC and HAPs information by company, location or department.

IMTEK Environmental
onlinemsds.com

SPRING-LOADED CONNECTORS

High-density, 0.050" pitch through-hole and surface mount spring-loaded connectors come in single and double-row strip packaging. Spring pin components are plated with 20 µm hard gold and assembled in a high-temperature thermoplastic insulator suitable for wave and reflow soldering processes. RoHS-compliant.

Mill-Max
mill-max.com

EMC SUPPRESSION SHEETS

Flexield family of IRJH3 magnetic sheets suppresses electromagnetic noise radiated by ICs and flexible PCBs, especially at frequencies of 500 MHz to 2 GHz. Original soft magnetic materials and polymer materials were combined to create a magnetic powder. Reportedly attenuates noise at frequencies from 10 MHz to 3 GHz. Has a certified flammability rating of UL94V-0.

TDK-EPC
tdk-epc.us

LED PLACEMENT

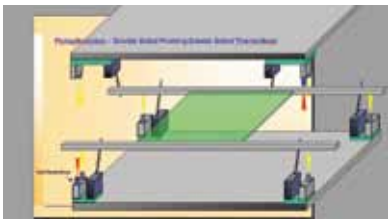
JX-100LED supports boards up to 31.5" x 14" when indexed twice in the machine. Features new algorithms for placement of side-view-type LEDs, top-view LEDs, rectangular ferrite chip-type and PLCC-type LEDs. Supports automatic tool changer. Places a reported 15,300 cph at IPC-9850; handles parts from 01005 to 33.5 mm^2. Features optional tri-colored vision centering system for placing fine-pitch QFPs, BGAs and QFNs.

Juki Corp.
jukiamericas.com

DRY CABINETS

MSD 1200 Series offers access from two sides that can be expanded to meet production needs and a new dry unit with closed-loop on-demand regeneration. Said to exceed IPC J-STS-033B.1 requirements for handling MSDs. Zeolite dryers feature dehumidification, reportedly reducing RH of an MSD1212 from 50% to less than 5% in 240 sec. under unloaded conditions at 25°C. Optimal humidity levels are below 0.5% RH. Regenerates only when necessary.

Totech Superdry
totech.eu.com



FLYING PROBE TEST SENSOR

ThermoScan can be installed on a flying probe shuttle for general application or a probe module with Z-movement for more accurate measurement over ICs. Provides troubleshooting information for PCB repair. Measures and analyzes thermal behavior of single-sided and double-sided PCBs. Temperature range -18° to 220°C; measurement accuracy 3%.

Acculogic Ltd.
acculogic.com

OTHERS OF NOTE

'HIGH-OPEN TIME' PASTE

RMA250 solder paste is a rosin-based chemistry designed to provide a high level of repeatability and consistency. Reportedly offers excellent open time, abandon time, and soldering activity with all surface finishes. Is formulated for fast printing and meets J-STD-004, -005 and Bellcore. Is low voiding. Post-process residues are clear and can be removed with a saponifier.

FCT Assembly
fctassembly.com

REFLOW OVEN CLEANER

Formulated micro-emulsion solvent removes all types of flux residues from reflow ovens and wave solder machines. Is nonflammable, low toxicity and low odor. Is said to prevent buildup of condensed flux residues. Can be used at temperatures of 20°-50°C, with an optimum working temperature of 40°C.

Electrolube
electrolube.us.com

LED TRACKING

LED BIN validation and traceability software validates SMT line setup by tracking each reel to its feeder and specified feeder location on the machine; ensures each replacement reel contains LEDs with a correct and compatible brightness index number. Generates traceability reports based on the BIN of each LED reel used. Stops machine when process validation error occurs.

Cogiscan
cogiscan.com

DDR3 CONNECTIVITY VALIDATION

ScanWorks toolkit for embedded instruments validates connectivity of DDR3 memory chips with certain Intel processors. Verifies performance of the bus that connects DDR3 memory to Intel processors based on the micro-architecture codenamed Sandy Bridge. Intel IBIST embedded instrumentation drives data patterns onto bus that connects processor to DDR3 devices.

Asset InterTech
asset-intertech.com

PANASONIC CM NOZZLE REPLACEMENT FILTERS

Cone-shaped XS filters are for Panasonic CM402 and CM602 nozzles. Come in packs of 100 and are designed for 100-series, 100S-series, 200-series, 200S-series, 400-series and 1000-series nozzles. Are compatible with Panasonic replacement nozzles for high-speed (8- and 12-nozzle, Type A-0 and A-2) and multifunctional (Type B) placement heads.

Count On Tools
cotinc.com

SELECTIVE SOLDERING ROBOT

BR 300 is based on four numerical axes for the automation of bottom-side selective point-to-point or linear iron soldering operations. Enables soldering tasks of through-hole components without complex handling. Components can be placed automatically. Performs placement and soldering operations rapidly.

MTA Automation
mtaautomation.com

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In Case You Missed It

This column provides abstracts from recent industry conferences and company white papers. With the amount of information increasing, our goal is to provide an added opportunity for readers to keep abreast of technology and business trends.

Solder Materials

"New Developments in High-Temperature, High-Performance Lead-Free Solder Alloys"

Author: Anton-Zoran Miric; anton.miric@heraeus.com.

Abstract: This paper reviews the composition, hardening mechanisms and performance of a new SAC metallurgical system. The alloy has small amounts of antimony, bismuth and nickel that harden the alloy and improve creep strength, resulting in significantly improved reliability (vs. SAC and SnPb) of solder joints at standard temperatures of 125°C, especially with ceramic chip components. This alloy enables operating temperatures of up to 165°C. (SMTA International, October 2010)

Solder Reliability

"Low-Silver BGA Assembly Phase II – Reliability Assessment Sixth Report: Thermal Cycling Results for Unmixed Joints"

Authors: Dr. Gregory Henshall et al; greg.henshall@hp.com.

Abstract: Some BGA suppliers are migrating sphere alloys from SAC 305 (3% Ag) or SAC 405 (4% Ag) to alloys with lower-Ag contents. There are numerous perceived reliability benefits to this move, but process compatibility and thermal fatigue reliability have yet to be fully demonstrated. The current study was undertaken to characterize the influence of alloy type and reflow parameters on low-Ag SAC spheres assembled with backward and forward compatible pastes and reflow profiles. This study combines low-silver sphere materials with SnPb and Pb-free SAC 305 solder pastes under varied reflow conditions. Solder joint formation and reliability are assessed to provide a basis for developing practical reflow processing guidelines and to assist in solder joint reliability assessments. This, the sixth report in a series, presents thermal cycling results. Thermal cycling conditions include 0° to 100°C and -40° to 125°C, with 10 min. dwell times. Accelerated thermal fatigue reliability of Pb-free solder joints with varying silver and "micro alloying" element concentrations is compared with that of 100% SnPb joints for four different package types. The impact of thermal cycle conditions on the rank order of the reliability for the different solder joint compositions is presented. Implications of the data regarding the efficacy of using BGAs balled with low-Ag alloys, and areas for future work, are discussed. (SMTA International, October 2010)

Screen Printing

"Stencil Technologies for Small Aperture Printing"

Author: Kevin Liticker; ksliticker@ra.rockwell.com.

Abstract: Balancing different paste volume requirements within the same stencil often requires the stencil designers to choose between optimizing stencil design for large parts, which can lead to poor print quality on the very small apertures, and optimizing for the small parts, which will starve the large parts of the necessary paste volume for a complete solder joint. A variety of stencil technologies purportedly reduce the acceptable area ratio well below the standard 0.66 limit, with the correct choice of materials and/or aperture forming (cutting) methods. This work evaluated several of these stencil technologies and aperture forming methods as they relate to paste transfer efficiencies for small apertures, including "PhD," fine grain stainless and nickel stencil methods, and pulsed YAG laser, fiber optic laser (with and without electropolish) and electroform forming methods. (SMTA International, October 2010)

Surface Finishes

"Silver Corrosion in Hugh Sulfur Environments"

Author: James S. Tonge; jim.tonge@dowcorning.com.

Abstract: The results of several studies on the behavior of silicone-coated silver substrates exposed to sulfur-based industrial pollutants, including continuous corrosion rate monitoring of silver circuits on glass substrates. An accelerated exposure tool was used to derive the controlling parameters in circuit performance in a mixed gas (H_2S, NO_2 and Cl_2) atmosphere at constant temperature and relative humidity. This work confirms that controlling the interface between the metal and silicone is a key factor in long-term silver corrosion protection. (SMTA International, October 2010)

Designer's Notebook, continued from p. 22

corner" land shape. Corner radius lands also improve the Pb-free solder process, but are good for both lead and Pb-free solder techniques. The corner radius used for the Least environment land is 0.05 mm.

Land pattern dimensions:

- C1 and C2 = center of component to center of land.
- Y1 and Y2 = land length.
- X = land width.
- R1 and R2 = silkscreen outline.
- V1 and V2 = placement courtyard excess.

See **FIGURE 2** for the "Nominal" environment dimensions. The corner radius used for the Nominal environment land is 0.1 mm. See **FIGURE 3** for the "Most" environment dimensions. The corner radius used for the Most environment land is 0.15 mm. The difference in the land area versus component size is clear: The Most environment is too robust for this component.

The 0603 (EIA 0201) component is so small that in all three environments, the land heel must be auto-trimmed to maintain the minimum 0.2 mm (0.008") land-to-land spacing rule. If the Nominal environment normally is used, my recommendation for chip components smaller than 1.0 x 0.5 mm (metric 1005, or EIA 0402) is to use the Least environment. If the Most environment is normally used, use the Nominal environment for those chips. PCD&F

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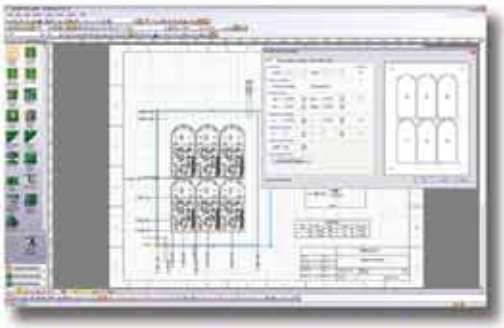

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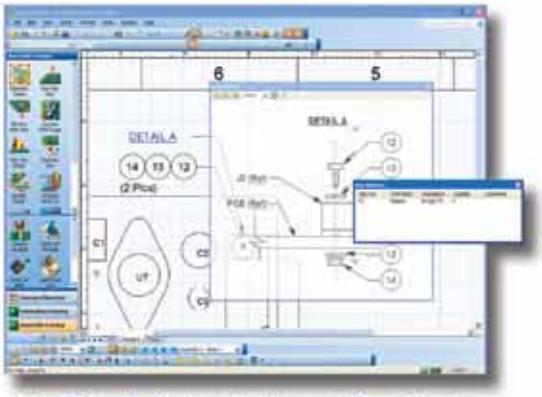

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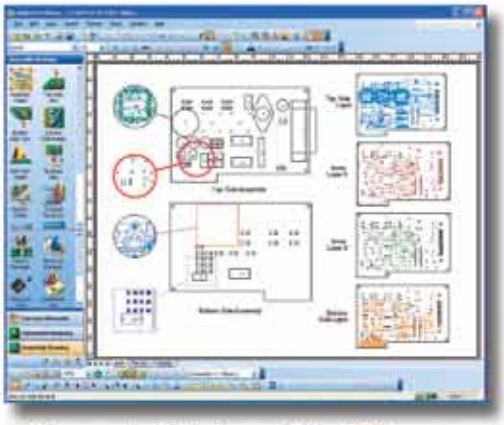

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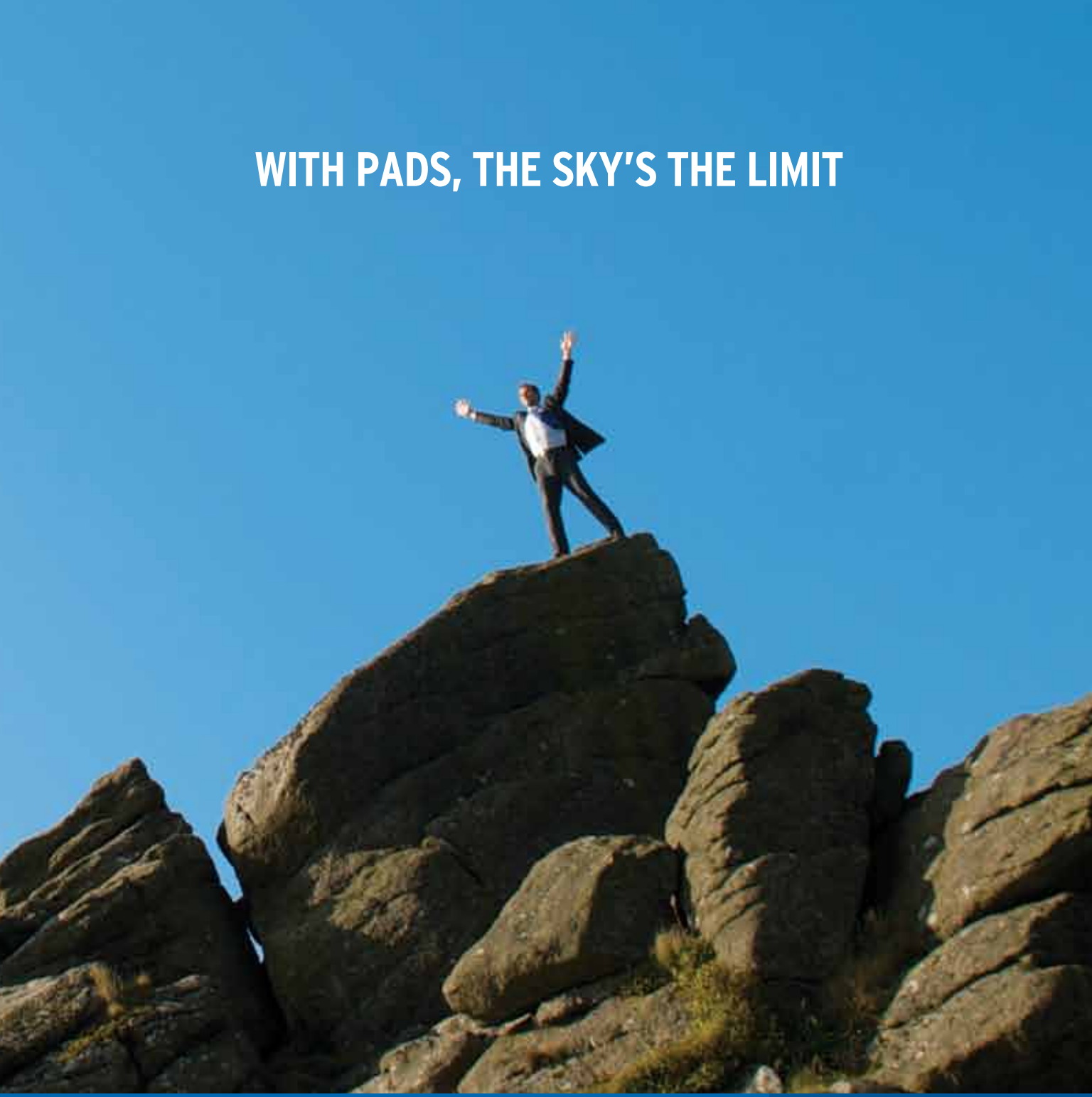

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