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GEDMS Brings High Speed, High Reliability and High Maintainability to Critical Control Systems

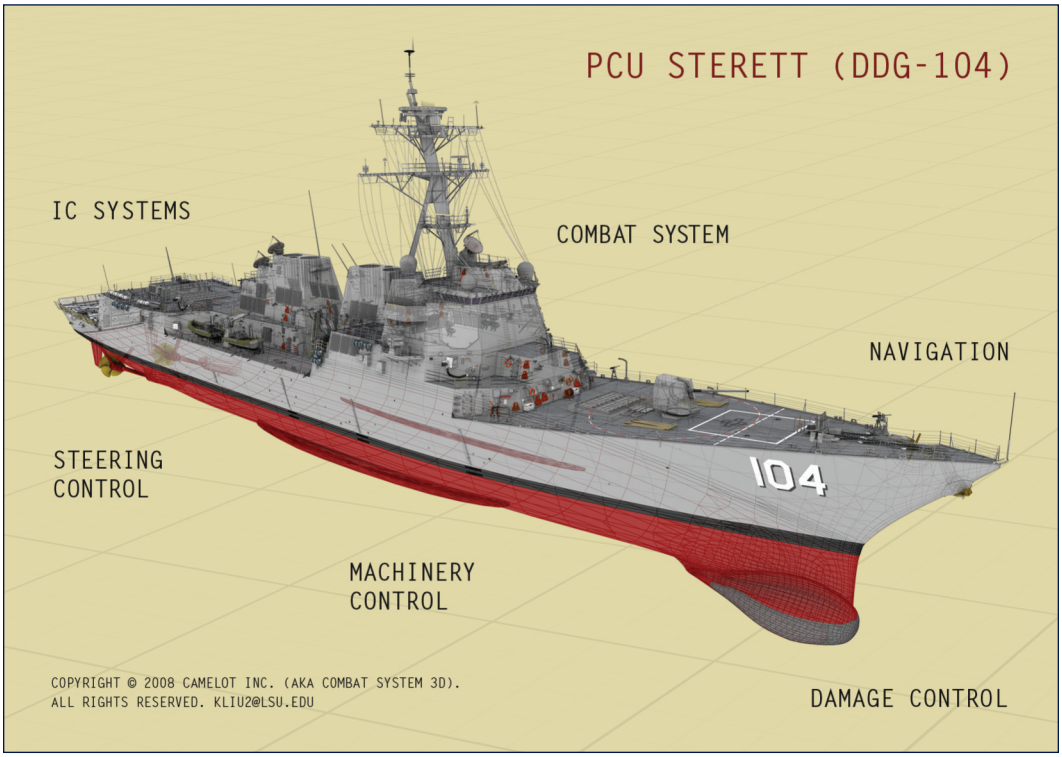

Figure 1-1: Control systems operating over DMS (Courtesy of The Boeing Company).

The Gigabit Ethernet Data Multiplex System (GEDMS) is a DDG51 mission-critical, ship-wide data transfer network for the machinery control system, damage control system, steering control system, AEGIS Combat System, navigation displays, and interior communication alarms and indications. For over 20 years, the most expensive component in the input output unit (IOU) for GEDMS has been the flexible circuit assemblies. The cost of these assemblies comprises over 30 percent of the total cost of the unit. With the recent addition of gigabit Ethernet interface capability to the IOU, there is dire need for updating the flex cable assemblies to support the higher signaling rates. Under this Navy ManTech project, the EMPF will leverage Boeing's investment in manufacturing enhancement work to develop flexible circuit assembly prototypes for performance validation and inclusion in the government's production design package. The introduction of these prototypes into the IOU will improve performance and lower acquisition, installation and total ownership costs.

The Data Multiplex System (DMS), AN/USQ-82(V), the first ship-wide control system network installed in a U.S. Navy ship class, was introduced in the mid-1980s primarily as a means of significantly reducing point-to-point cable runs by multiplexing signals on a common networked infrastructure. The Arleigh Burke

continued on page 2

Message from the Director

The Electronics Manufacturing Productivity Facility (EMPF) has a track record of providing technology assessments for the Navy that entail nearly all elements of electronics manufacturing technologies. The EMPF uses technology roadmaps from trade organizations and research consortia, assessments of the technology maturity via current government and industrial definitions for TRLs and MRLs, and assessments on how the manufacturing or electronics technology aligns with industry standards and best practices. The objective of the assessments is to determine and predict the relative success the technology has in reaching maturity and what will be required to achieve maturity and the acceptance of the technology by the electronics industry which will directly determine the availability and affordability of the technology to the Navy when it is needed.

The EMPF has generated innovative investment recommendations that have created transformational improvements in affordability, supportability, and performance on key platforms within the Navy ManTech Strategy. These investment recommendations were developed through a proactive involvement and strong relationships with acquisition PMs and industry partners. The EMPF has developed and maintained relationships with most major SYSCOMS and PEOs sufficient to understand their priorities and ensure that transitions are being planned and executed. The quality of these recommendations have either met or exceeded the Navy's expectations as evidenced by direct feedback from the weapon system stakeholder.

Through resource leveraging, the continued use of proven and effective processes, and the introduction of new and innovative strategies, the Electronics Manufacturing Technology COE will remain at the forefront of manufacturing technology innovation and maximize Navy ManTech's return on their critical technology investments.

Michael Frederickson

GEDMS Brings High Speed, High Reliability and High Maintainability to Critical Control Systems

(continued from page 1)

(DDG 51) Class of guided missile destroyers was the first to include a control system network in the baseline design. From the beginning, many of the ship's major systems – machinery control, damage control, interior communications and alarms, and combat system navigation were designed to utilize the DMS (Figure 1-1). The presence of a network in the ship design permitted flexibility in establishing the design baseline, reducing the integration risk to the shipbuilder/integrator, while allowing future enhancements to be incorporated in the ship design with low risk at a later date. At the same time, DMS allowed for simpler system reconfiguration, even during the design process, because signals could be re-routed without changing the physical cable plant of these ships. [1]

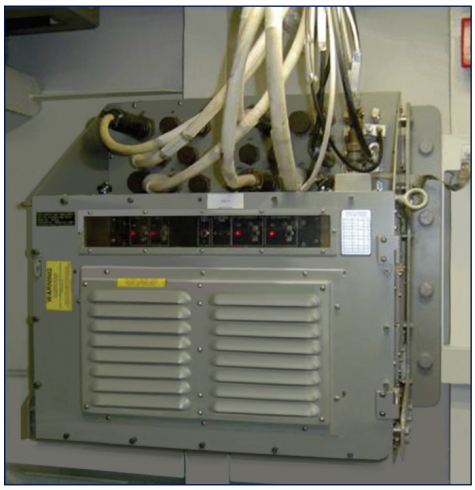

Figure 1-2: AN/USQ-82(V) IOU installed on Arleigh Burke-class DDG (Courtesy of The Boeing Company).

The next improvement for DMS was the introduction of a fiber optic backbone (FODMS). This changed the internal system protocols from fast circuit switching to true packet switching. This allowed simpler, lower cost commercial network hardware and extended the backbone speed from 24 Mb/s of DMS to 100 Mb/s.

The current DDG-51 class modernization program includes the third DMS network backbone upgrade, GEDMS, which further increases the backbone speed to 1 Gb/s. The FODMS/GEDMS network is a complete information transfer system that enhances reliability, maintainability, and survivability by managing data from the ship's navigation, steering control, damage control, machinery control, combat, and internal communications systems. Currently, DMS/FODMS is installed on 45 percent of naval surface combatants and 34 percent of all surface ships. With the addition of GEDMS, shipboard networking will be present on 65 percent of naval surface combatants and 42 percent of all surface ships. The Design Agency contract for Data Multiplex System (DMS) and FODMS/GEDMS is managed by Boeing's Network and Tactical Systems Division headquartered in Huntington Beach, CA. This organization also provides GEDMS production capability.

While the new gigabit Ethernet modules can operate at a 1,000 Mbit/sec link speed, the existing flexible circuits introduce an impedance discontinuity interface that limits the performance to a 100 Mbit/sec link speed. The continual upgrade of the Navy's equipment to Internet Protocol (IP) based interfaces is driving the need for the higher data rate interfaces to the GEDMS IOU equipment. Hence, there is an urgent need to

continued on page 3

GEDMS Brings High Speed, High Reliability and High Maintainability to Critical Control Systems

(continued from page 2)

develop a cost effective and producible IOU flex cable solution that meets the performance requirements.

Figure 1-2 is a picture of the IOU hardware as installed on an Arleigh Burke-class destroyer. Flex cables provide electrical interface between circuit cards and external connectors. Figure 1-3 is an image of an IOU with the rear cover removed, showing the installation of the 15 flexible circuits.

The goal of this ManTech project is to integrate three seemingly conflicting requirements into a single cost-effective packaging solution: 1) moderate current carrying capacity; 2) high circuit impedance (100 Ohms desired for Gigabit Ethernet signals); and 3) cost-effective assembly and packaging techniques. Modern circuit board design techniques will be used to accomplish the first two objectives. The third objective will be addressed by modifying the design to utilize easily repeatable and transportable processes, as well as reducing touch labor in the manufacturing process.

This effort requires a balancing of the technology used to produce the flexible circuits with the objective to reduce the "touch labor" associated with the assembly of these parts wherever possible and to select the flexible circuit structure that provides the necessary performance at the lowest cost.

Powerful impedance modeling software was used to evaluate the competing design requirements and constraints of controlled differential impedance and high current. The optimum trace width, height, and separation were determined for a new rigid-flex circuit design. Connectors and hardware were also evaluated for cost effective replacements with the least risk and highest yield. A manufacturing best practice assembly and packaging guideline document will be produced to describe this design phase. Once the detailed design is approved, the fabrication and validation of the first prototype will occur.

The GEDMS IOU contains 15 distinct flex circuit assemblies. Eleven use a 42-pin M28840 connector to provide an interface to the external user systems and four use a 92-pin connector to interface to the external user systems. While the user systems connected to the 92-pin connectors would not benefit from the higher interface speeds, assembly modifications discovered during prototyping the 42-pin assemblies will be considered for incorporation into the four 92-pin if they reduce the production costs. The completed prototypes will be evaluated for performance and fit in an actual GEDMS IOU.

This Navy ManTech project directly matches the Navy fleet priority of affordability and is specifically applicable to the DDG Modernization program. Incorporation of these design and manufacturing updates will improve the performance capabilities of the IOU, while reducing acquisition and installation cost. Improving the capability of the GEDMS input output unit and using this on other ship classes would reduce life cycle costs and provide alternatives for obsolescence issues.

The EMPF continues to be an active partner in the Navy's ship building affordability initiative by developing projects that reduce the acquisition costs of shipboard electronics through the introduction of advanced manufacturing processes, improved electronic devices, materials, and system technologies. Expanded use of COTS, open systems, and an increased use of electronic functional integration will be applied to ship board systems resulting in substantial savings to the Navy.

For more information about the EMPF Center of Excellence and Navy ManTech Projects, contact the EMPF Helpline at 610.362.1320 or email helpline@empf.org if you have any questions.

Reference:

[1] Meier, Scott, and Thomas Morris. "Gigabit Ethernet Data Multiplex System (GEDMS) - Supporting the Modernization of Navy Combatants." Automation & Controls Symposium 2007. IP Hotel & Casino, Biloxi, MS. American Society of Naval Engineers (ASNE), 11 Dec. 2007.

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Figure 1-3: One of the flexible circuits in AN/USQ-82(V) IOU that will be redesigned to achieve gigabit Ethernet speeds (Courtesy of The Boeing Company).

ALD Successfully Used as Conformal Coating for Radar Components

The United States Navy plans to use advanced and integrated electronics in future radar platforms as the means to achieve transformational capability. These goals will include the development of less expensive, more easily applied, more reliable, and more moisture proof conformal coatings for radar electronics. Of particular interest is the Atomic Layer Deposition (ALD) ceramic based coating that has the potential of providing hermeticity to these electronics. Significant savings are expected from avoidance of the heavy, bulky, hermetic ceramic packaging currently used for this application, by coating the MMIC chips before packaging, or by coating the completed electronic assembly using these ALD-based coatings.

The important attributes of ALD hermetic coating to be harnessed in this project are:

- To achieve equivalent hermetic performance, without expensive and heavy hermetic ceramic packaging, that enables the use of the less expensive plastic materials and surface mount processes
- To supply sufficient moisture resistance and hermeticity with a chip level ALD coating, applied in the chip foundry environment, that enables larger cost reduction, and potentially better MMIC performance than initially anticipated

The benefits of this project include:

- Passing military radar environmental screening tests with a chip level ALD coating that provides sufficient hermeticity for radar structures
- Reducing labor hours and material costs associated with skilled, labor-intensive fabrication of conventional hermetic ceramic packaging
- Reducing the labor and material costs of achieving plastic-based but equivalent hermetic radar packaging

The ALD for Radars ManTech project showed that two defense contractors could successfully use ALD with their radar components and modules with only minor, acceptable variations in RF performance due to the coatings.

This article summarizes the ALD process; how ALD is used in a manufacturing process; and discusses some lessons learned in measuring thicknesses of the films, masking areas where ALD isn't desired, and dealing with rework.

Background

Atomic layer deposition is a thin film deposition process in which the film is built layer by layer through sequential exposures to reactive chemical vapors. Extensive reviews have been produced that go into detail on ALD and a variety of applications. [1]

An ALD film is grown by repeating the following steps:

1. Exposure of the first precursor
2. Purge/evacuation of reaction chamber – removes non-reacted precursors
3. Exposure of the second precursor
4. Purge/evacuation of reaction chamber

ALD processes have also been called Binary Reaction Sequence (BRS), Atomic Layer Epitaxy (ALE), Molecular Layer Epitaxy (MLE), and Atomic Layer Chemical Vapor Deposition (ALCVD).

The surface of the substrate being coated must have chemical functional groups that will provide attachment points for the film. By using surface reactions that are self-limiting, the two reactions can deposit a thin film with atomic level control. ALD is documented to produce highly uniform, conformal, defect-free, crack-free, and pinhole-free thin film growth both on large area substrates and challenging nano-architectures.

ALD can also deposit a wide range of metal oxides, nitrides, metals, organic polymers, and combinations thereof, which include nanolaminates, graded layers, mixed oxides, and doped thin films, which can be used in numerous applications in the semiconductor and IC (integrated circuits) industry.

Manufacturing Process Development

The ALD process development has been fairly limited since the ALD equipment suppliers provide turnkey systems. Most of the effort has been spent understanding what the controlled variables are, what the available options are and why one may be preferred over the others. The vendors (Sundew Technologies and Cambridge NanoTech) define and control the variables that most affect the ALD process. These include the chemical set being used, the processing temperature, flow rates, injection/purge times (for H_2O and reagents) and number of cycles. Identified variables which are not controlled by the vendor include the package geometry, construction materials, part cleanliness, ambient humidity and pressure and operator.

The module that was coated was a representation test vehicle. To date no envelope test had been performed to see what feature sizes (depth of cavities, amount of organic material, size of part) affect the process.

During the initial ALD coating operations, more variability in coating thickness was experienced than was expected. Part of the variability appeared to come from the complexity of the part geometries, and some of it was thought to be a result of precursor chemical interaction or chamber volume interaction with flow and purging. One critical set of experiments, looking at ALD thickness repeatability over time, needs to be completed. Once the size of the chamber is determined and the cycle timing and number of cycles are locked down, the coating thicknesses is expected to become more repeatable. As the process becomes more repeatable, the uncontrolled variables will

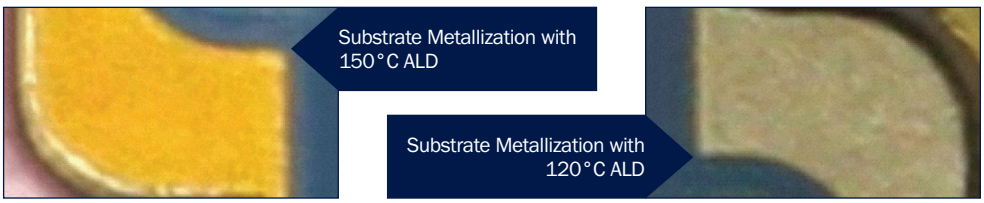

Figure 2-1: ALD Color Variation with Respect to ALD Chamber Temperature

continued on page 5

be more closely examined. What affect local geometry, part cleanliness, room cleanliness and ambient conditions have on coating thickness and uniformity will need to be determined.

The most limiting potential variable (for both vendors) was processing temperature. The use of ALD coating as a protective layer over the assembly requires that the assembly be complete prior to coating. Most electronic assemblies are built in various stages of temperatures (such as package brazing at 300+°C, SnPb soldering at ~200°C, epoxy cures at 150°C). Depending on assembly sequence and geometry, electronic assemblies have varying tolerances for temperatures above 120°C. SnPb solder joints will see significant metal migration at temperatures of 150°C for times exceeding one hour. Both vendors of ALD equipment typically run their chambers at over 200°C. Those temperatures would be detrimental to completed micro-electronic assemblies typical in radar module production. For one subset of ManTech testing: Au based LTCC parts were coated with 200 nm of Al_2O_3/Al_2TiO_5 and Al_2O_3/ZrO_2 at 120°C; the other subsets: Ag based LTCC parts and HTCC parts, were coated with Al_2O_3/ZrO_2 at both 120 and 150°C to a thickness of 100 nm. The degree to which the processing temperature affects the protective quality of the coating will need to be determined; early HAST results could indicate both 120 and 150°C ALD coatings can pass HAST (with a sample size of only 1 each). If the coating must be done at 150°C, that will restrict the amount and type of SnPb solder that can be used on the assembly prior to ALD coating. If the ALD coating is successful at 120°C, then the number of designs that can be coated will increase. A noticeable color difference was evident on the parts after Al_2O_3/ZrO_2 between the 120 and 150°C. The 150°C coated parts exhibited a darker yellow tint/hue, while the 120°C coated parts still exhibited a yellow tint/hue but not as dark. An example of this color difference is shown in Figure 2-1.

Quality Issues

There were two primary process measurement techniques identified. Sundew used the change in color of a standard color chip to ensure proper ALD coverage. While the technique was very fast and easy to perform, it lacks the rigor required for a process control. Another option was to pot, cross-section, and measure the thickness using the scanning electron microscope (SEM). This technique yields very precise measurements, but is limited to small areas of the part, and is destructive. Cambridge recommended the use of witness wafers. After coating, an ellipsometer was used to measure the coating thickness. This technique did not measure parts directly and required multiple test locations per run. By coupling the two processes (preliminary cross-sections to correlate test wafer measurements to coating thickness on parts, and using the color shift to look for uniformity), sufficient process controls to ensure uniform coating thicknesses were established. A statistical process control (SPC) coupon will be used to routinely measure the coating thickness at known positions within the chamber, along with an optical review of each part to verify application of the coating.

Most of the effort to date has focused on the impact of ALD on electrical performance and environmental protection. There does not appear to be a clear method to evaluate the peel strength of the coating. HAST and other biased humidity tests provide functional information about bond strength, but other procedures must be developed. The number of stacked coating runs (thickness) allowable for production hardware must be defined. Effective rework procedures must be developed to remove ALD. There is also a need to ensure that the environmental protection persists after handling.

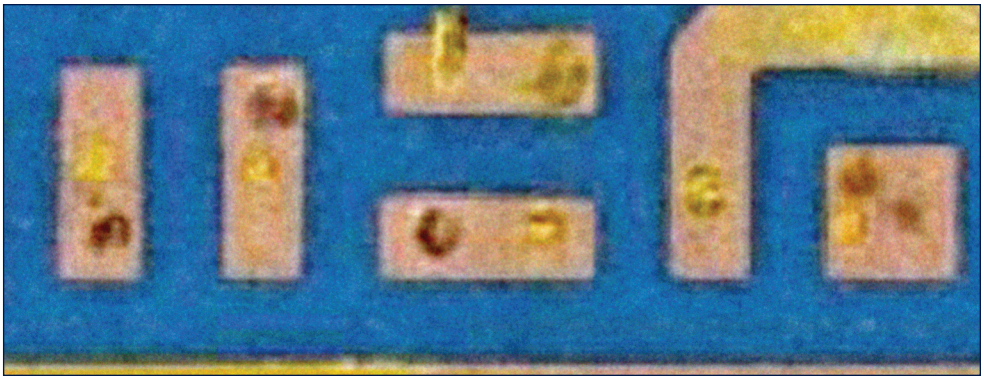

Figure 2-2: Chip pad after chip removal

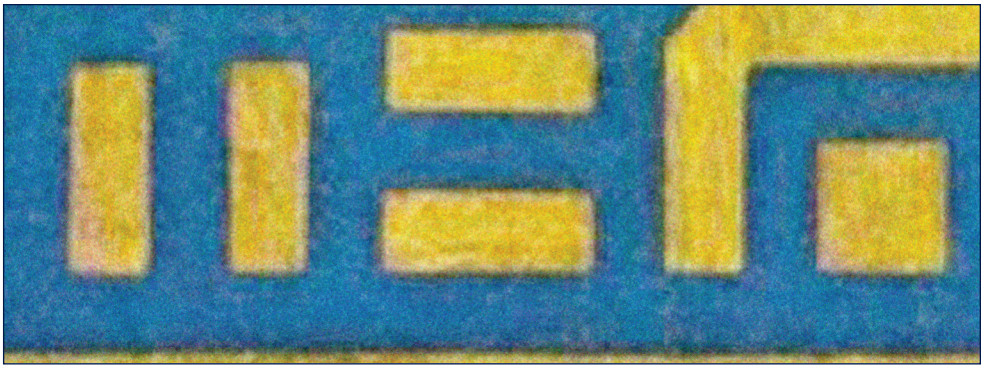

Figure 2-3: Chip pad after cleaning

Masking

Masking materials have been a significant area of study in a recent electronics manufacturing project. In the study, most of the assemblies were coated, but the connector interfaces that had to remain conductive. To stay conductive, the connector was required to remain free of the ALD coating.

Most of the materials studied outgassed in the high vacuum cycle of the ALD process. The outgassing caused fluctuations in the film

continued on page 6

thickness, sometimes preventing it in a localized area. The outgassing is a consideration, not just for masking materials, but also for all organic materials used in an assembly to be coated.

Table 2-1 summarizes the masking techniques that were evaluated. The analysis began with a thinned photoresist, which had several issues in the production process. While it was effective at preventing the ALD coating, it was time consuming to position accurately and was difficult to completely remove. Once coated with ALD, the photoresist was protected and difficult to remove. There were also materials used for masking in Parylene processes. The latex solder mask was easy to apply and remove, but reacted with the ALD application process and caused a thinner coating near the mask. This was also observed when using Kapton tape. Flash breaker tape is a thick, high-temperature resistant, polyester tape used in the aerospace, composites, and electronics industries. The flash breaker tape didn't affect the ALD coating, was easy to apply, and was not difficult to remove.

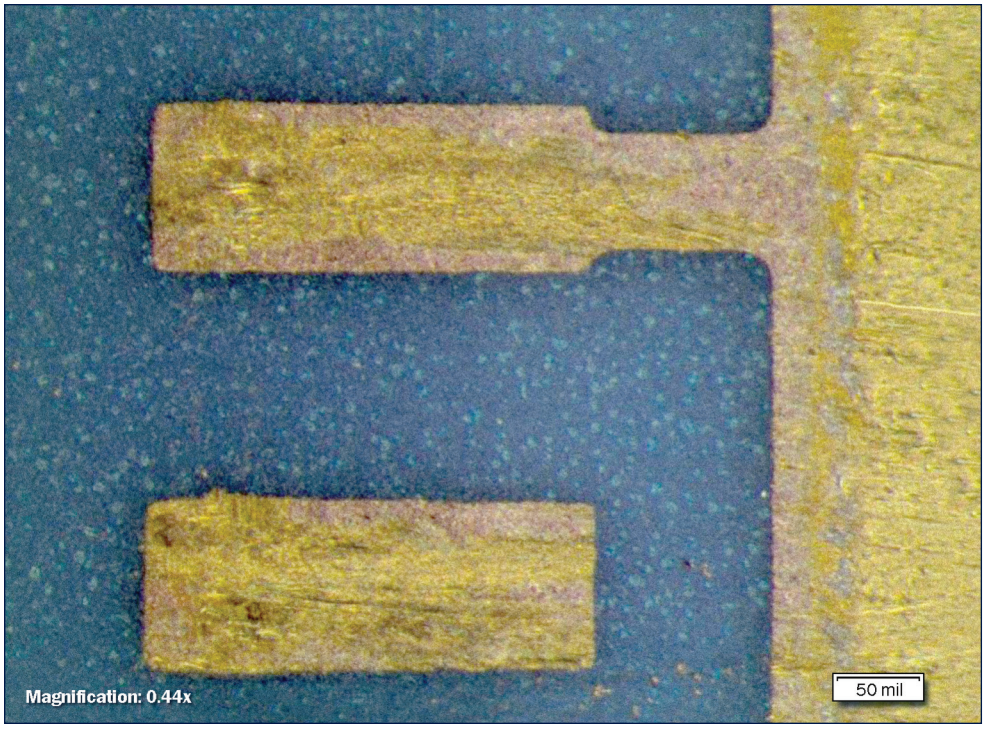

Figure 2-4: Detail of wire bond pad after cleaning

Material	Ease to Apply	Ability to Remove	Impact on ALD
Teflon Tape	+	+	+
Kapton Tape	+	=	–
Flash Breaker Tape	+	=	+
Latex Solder Mask	=	=	–
Photo Resist	–	–	+

Table 2-1: Masking Material Comparison

Note: The green plus signs (+) indicate a positive result; red minus signs (–) indicate a negative result; and the equal signs (=) show no particular advantage and no detrimental impact.

Teflon tape on the connector's contact areas, held in place with mating connectors, functioned well as a mask. This provided a repeatable masking process with the smallest cost impact. It was quick to apply, removed completely, kept the mating surfaces free of the ALD coating, and did not interfere with the application process.

Rework

A brief review was performed of standard rework processes applied to ALD coated modules to address the ability to rework parts that have been coated with ALD. The review included chip replacement and wire bond rework. ALD had virtually no impact on chip removal. Since the coating will not be present under chips or on replacement chips, the risk is very low for placing new chips on old sites. Chip replacements were performed and there was no impact from the ALD on the mechanical attach, epoxy cure, or vision system.

Although the ALD coating had no effect on chip removal, the cleanup after removal was difficult. Specifically, the wire bond pads around chips required a lot of extra work to remove the coating. Figure 2-2 shows a pad after chip removal and Figure 2-3 shows the same pad after cleaning. Take note of the edges of all pads. Due to the three dimensional nature of thick film metals, ALD was removed preferentially from the tops (centers) of pads and small amounts of ALD are left around the perimeter of pads.

Wire bonding to ALD coated areas posed a challenge of breaking through the ALD layer and insuring the gold underneath was very clean. As an alternative to bonding through the ALD coating, burnishing the bond pads breaks up the coating and exposes fresh metal for bonding. Generated particulates were not experienced as an issue. This technique will not work for coated chips, since one cannot burnish individual pads on the chip surface. If wire bonds need to be reworked without replacing chips, then a remnant of the old wire on the chip pad can be left to provide a

continued on page 7

ALD Successfully Used as Conformal Coating for Radar Components (continued from page 6)

clean gold spot for bonding. If wire cannot be left on the chip pads, the entire chip would need to be replaced. Figure 2-4 shows a detail of wire bond pads on ceramic. The centers of pads will accept new bonds without issue.

Rework Conclusion

While reworking an ALD coated module will require slightly more clean-up work, it will not affect the integrity of the module. After rework operations were complete, the intent was to recoat the entire module with ALD. The implications of multiple ALD coatings were not explored. Items that should be investigated include: looking at ALD adhesion to previously deposited ALD, maximum thickness for aggregate coatings, RF impact of thicker ALD, and the impact of multiple mask/de-mask cycles.

Summary

Methods for incorporating ALD into electronics manufacturing at the module level were developed, including parameters such as: temperature considerations; coating thicknesses and inspection criteria; masking methodologies and materials; and rework processes.

ALD holds great promise for a variety of applications, and with these lessons learned, further development could be accomplished.

For more information on the benefits of ALD, please contact the EMPF Helpline by telephone at 610.362.1320 or email helpline@empf.org.

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[1] George, Steven M. "Atomic Layer Deposition: An Overview." *Chemical Reviews* 110.1 (2010): 111-31. American Chemical Society, 30 Nov. 2009. <http://chem.colorado.edu/georgegroup/images/300.pdf>.

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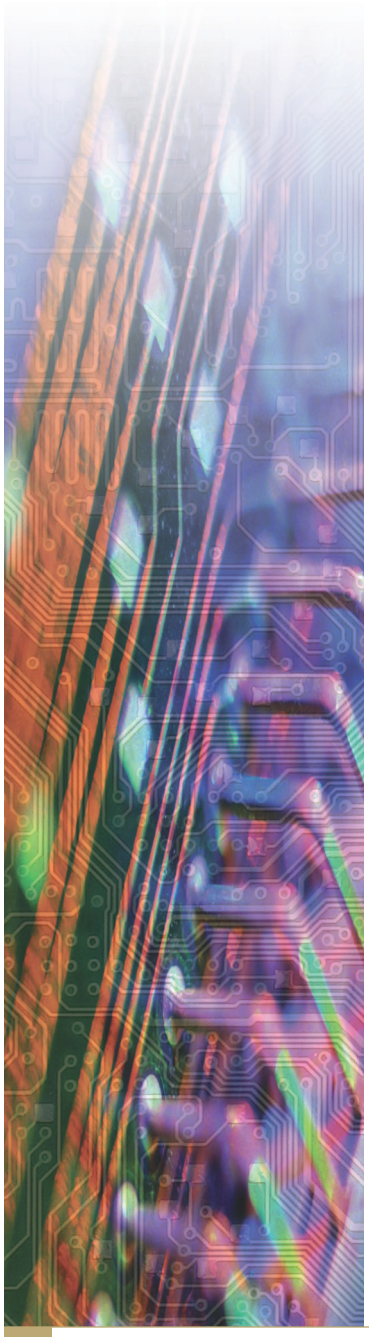

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