empfasis

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Michael D. Frederickson,
EMPF Director

Barry Thaler, Ph.D. • bthaler@aciusa.org
EMPF Technical Director
Empfasis Technical Editor

Paul Bratt • pbratt@aciusa.org
Empfasis Editor

In this Issue

ACI Technologies, Inc.
One International Plaza, Suite 600
Philadelphia, PA 19113
610.362.1200 • *fax:* 610.362.1290
Helpline: 610.362.1320
web: www.empf.org • www.aciusa.org

Properties of Low Dielectric Constant Laminates

There are several attributes to be aware of when considering high frequency laminate materials which have low dielectric constant (Dk). Several key attributes and how they relate to reliability, manufacturability and good predictable electrical performance will be discussed.

Polytetrafluoroethylene (PTFE) based substrates are used to provide a laminate with a Dk that is relatively low (<2.5 for example). While PTFE has very good electrical properties, other properties need to be well understood for several considerations. The impact of Coefficient of Thermal Expansion (CTE), Thermal Coefficient of Dielectric Constant (TCDk), low modulus, and non-wettability will be discussed.

The RT/duroid 5870 and 5880 are low loss laminates that have been in use for decades. While both have a relatively high percentage of PTFE, the addition of a small amount of filler and some special processing reduces the x-y axis CTE to the range of 40 ppm/ºC (from the 300 ppm/ºC of pure PTFE). Keeping the x-y axis CTE relatively low and near the CTE of copper (17 ppm/ºC) is beneficial for reliability. Even though the CTE is higher in the z-axis (thickness) direction (173ppm/ºC and 237ppm/ºC for the 5870 and 5880, respectively), these materials have been used in numerous high reliability applications for many years. In general, a simpler printed circuit board (PCB) construction, such as a microstrip, minimizes reliability concerns. If the PCB construction is also thin, the effects of CTE can be made negligible. Also, multilayer applications have used this material successfully when certain considerations are met. Again, keeping the material thinner is beneficial and making a hybrid construction using very low CTE materials with the RT/duroid 5000 laminate will minimize any reliability concerns. Often, the circuit design will use RT/duroid material for the critical electrical layers and then use lower CTE materials for the other layers.

These materials have some of the lowest values for Dk and dissipation factor (Df) in the market. When tested at 10GHz, the Dk of RT/duroid 5870 and 5880 is 2.33 and 2.20 and the Df is 0.0012 and 0.0009, respectively.

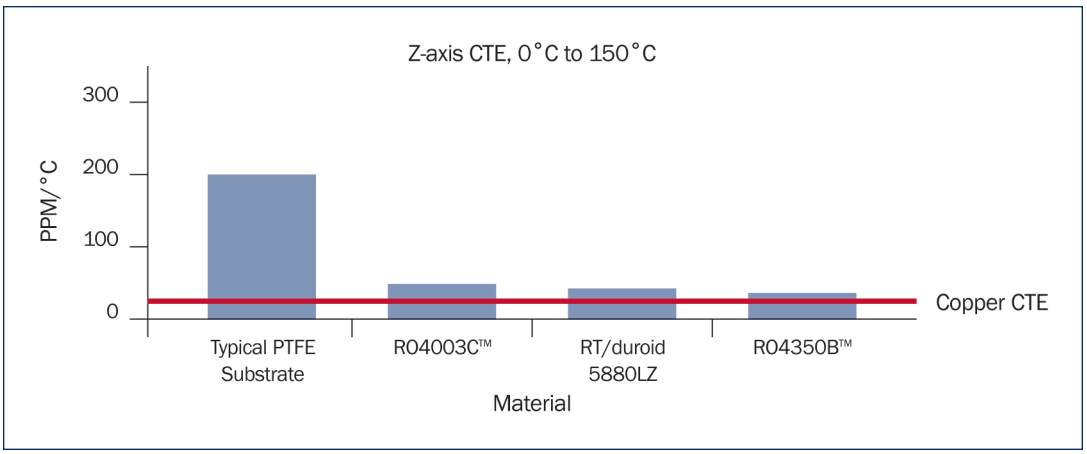

Figure 1-1: Comparisons of different high frequency laminates.

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Ask the EMPF Helpline!

Surface Finish Issues Affecting Solderability and Reliability

A customer recently contacted the EMPF helpline in regards to poor solder joint reliability.

The customer submitted an assembly that was exhibiting intermittent opens at multiple locations on a ball grid array (BGA) component. The assembly's functionality did not survive international shipping, essentially shock and vibration failures, immediately making the quality of the solder joints suspect. The customer was asked about the contract manufacturer and the reflow oven profile as well as the solder paste and surface finish used. The EMPF engineering staff evaluated the contract manufacturer's technique and determined that they were competent in the methods they used for placing thermocouples in the proper locations and developing the reflow oven profile. The surface finish was unusual, but not unheard of, in that it was hard gold over hard nickel, rather than electroless nickel immersion gold (ENIG). The customer was able to supply boundary scan testing data which showed a diagonal row of troublesome BGA pins.

The EMPF analytical services staff determined that cross-sectional analysis with optical microscopy and scanning electron microscopy (SEM) with energy dispersive X-ray spectroscopy (EDS) would provide the best information as to what had happened. The focus of the micro-sectioning was through the diagonal row of the BGA pins indicated by the boundary scan data.

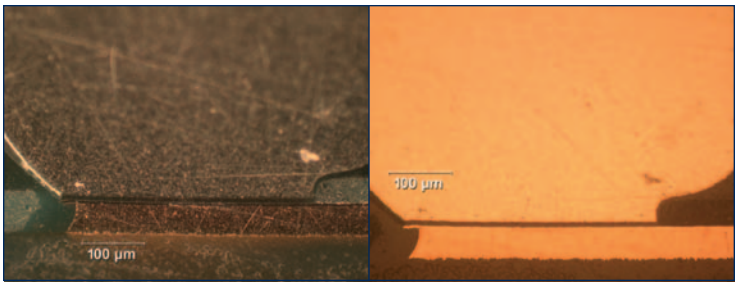

Figure 2-1: Optical images of a broken solder joint along the board pad to solder ball interface; dark field image on left, bright field image on right.

A position halfway through the BGA solder balls along a diagonal through the BGA component was selected as the area of interest to examine the solder joints, surface plating, and foil thickness as well as any anomalies from internal observations. The microsectioning was performed in accordance with IPC-TM-650 2.1.1 - Microsectioning, Manual Method. In Figure 2-1, images of one of the suspect solder joints are shown with a clean break along the board pad to solder ball interface.

After examining similar solder joint cracks under optical microscopy, the cross-section was analyzed using SEM-EDS. Figure 2-2 shows the pad interface of the cracked joint of an outer BGA solder ball in which nickel (Ni) was predominant with a minor contribution of tin (Sn). Figure 2-3 shows the solder ball interface of the same cracked joint of an outer BGA solder ball with copper (Cu) from the SAC (Sn-Ag-Cu) solder paste, nickel (Ni) from the pad, gold (Au) from the pad, and tin-silver (Sn-Ag) from the solder ball.

The low levels of gold observed at the interface, especially with no line of demarcation, and few intermetallics at the pad interface (with the hard gold over hard nickel plating) suggested that there was an issue with the bare board. Oxidation of the nickel plating, either during the surface finish deposition or through an insufficient layer of gold, could prevent solder from adhering to the pad to form a strong solder joint. The patchy intermetallic layer observed at the interface also suggested a blocking of the nickel interface.

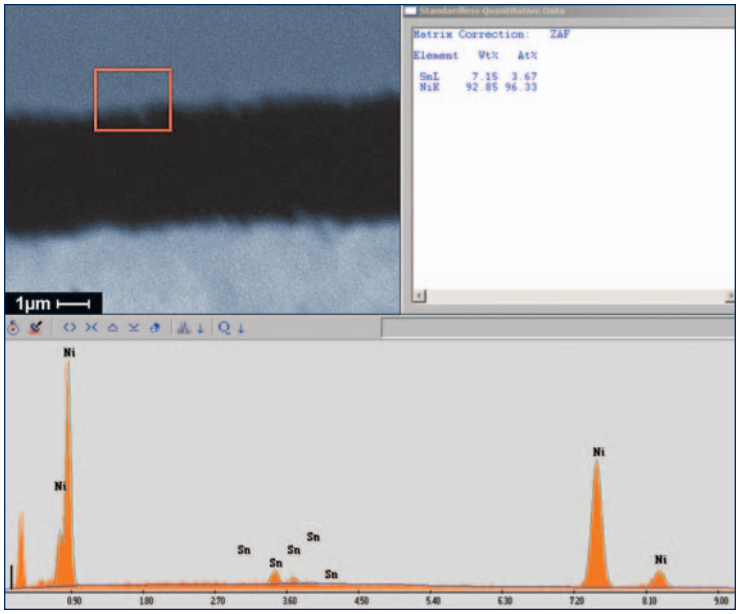

Figure 2-2: SEM-EDS data for the pad side of an outer solder joint that cracked.

The clean breaks at the nickel layer of some of the BGA solder joints, especially from the outside towards the inside of the component, indicated that it was less likely the assembly manufacturing process was the cause and more likely the bare board. During the reflow process, the corners of the component are the hottest and the center should be coldest. The center would most likely fail if the process was too cold while dewetting and excessive intermetallics would be observed if the process was too hot. This points to surface finish as the likely problem since low intermetallic formation was observed and the solder joints weren't broken near the center of the BGA.

The EMPF recommended evaluating the plating process of the bare board and the hard gold over hard nickel surface finish to see if they met the recommended thicknesses for the nickel and especially the gold layers. Also, removal of any storage or processing step that would have led to the oxidation or fouling of the nickel surface should increase the solder joint reliability.

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Conformal Coating Processes

In a previous *EMPFasis* article,[1] the main methods of conformal coating application were discussed. The EMPF can assist its users with process development and experimentation through the use of the conformal coating capabilities in the Demonstration Factory. Four types of coating processes are available at the EMPF: dip coating, manual spray coating, programmable spray coating, and manual brush application. (Manual brush application will not be discussed in this article.)

Manual spray coating is the most commonly used method at the EMPF. This type of application allows a wide variety of parts to be coated with minimal process development effort. A handheld spray coating booth, shown in Figure 3-1, is available and is regularly equipped with a silicone resin (SR) coating material. This booth has self-contained material and solvent storage tanks and pumping capabilities as well as variable coating pressure and flow rates. It also incorporates a large exhaust port to minimize build-up of flammable solvents during the spray process. The exhaust is filtered to prevent coating build-up in the facility exhaust infrastructure. These filters must be changed regularly as cured coating can build up on the filter material and reduce exhaust flow. The spray booth also contains a turntable to allow the operator to easily rotate the part undergoing coating while minimizing handling of the uncured coating.

The drawbacks to handheld spray coating are the difficulty in changing material types and the need to mask any areas where coating is not desired. This process does not allow the operator to avoid any areas on the assembly without risking inappropriate variation in applied coating thickness, so areas where coating cannot be applied must be masked. Masking techniques can vary, but the two most common are manually applied tape and mechanical fixturing. Each has its advantages and drawbacks. Manually applied tape has a low material cost, but the application is very labor intensive and can have variation in the areas masked from assembly to assembly. Fixtures are more costly but ensure consistent masking. They require regular cleaning of coating buildup and must be revised if significant changes are made to the design of the assembly.

Changing material types in the handheld spray coating booth requires significant effort to ensure all residual material is purged from the feed lines between the storage tanks and the spray gun. Residual material left in the feed lines can result in contamination of the new material, which could lead to inhibiting the cure of the new material or affect the ability of the material to adhere to the assembly.

The handheld spray coating booth can also be used for manual aerosol spray coating. This most commonly occurs when the EMPF is tasked to spray a small quantity of assemblies or where the risk of contamination is high from the SR coating normally used in the spray gun. This type of application leverages the advantages of the exhaust and turntable in the spray booth while avoiding the issues related to purging the old material from the system. The concerns about masking remain the same across both manual spray processes.

The EMPF also has a dip coating process available. This process is well suited for high volume applications with minimal coating type changes due to the amount of material required to fill the tank and initiate the process. The equipment at the EMPF has two separate tanks to allow for use of two different materials without the need to remove and discard large quantities of coating. The equipment allows for changes in the dip speed, the tank dwell time, and the removal speed.

The biggest disadvantage of a dip coating process is the use of open tanks of material. To reduce the risk from flammable solvent evaporation, the equipment at the EMPF uses a nitrogen blanket to inert the area just above the open tank where solvent buildup can occur. The exhaust system is also designed to evacuate any vapors that have accumulated. Additionally, the pot life of a coating in an open tank is significantly less than the unopened shelf life. This makes dip coating unsuitable for processes where coating is only occasionally performed.

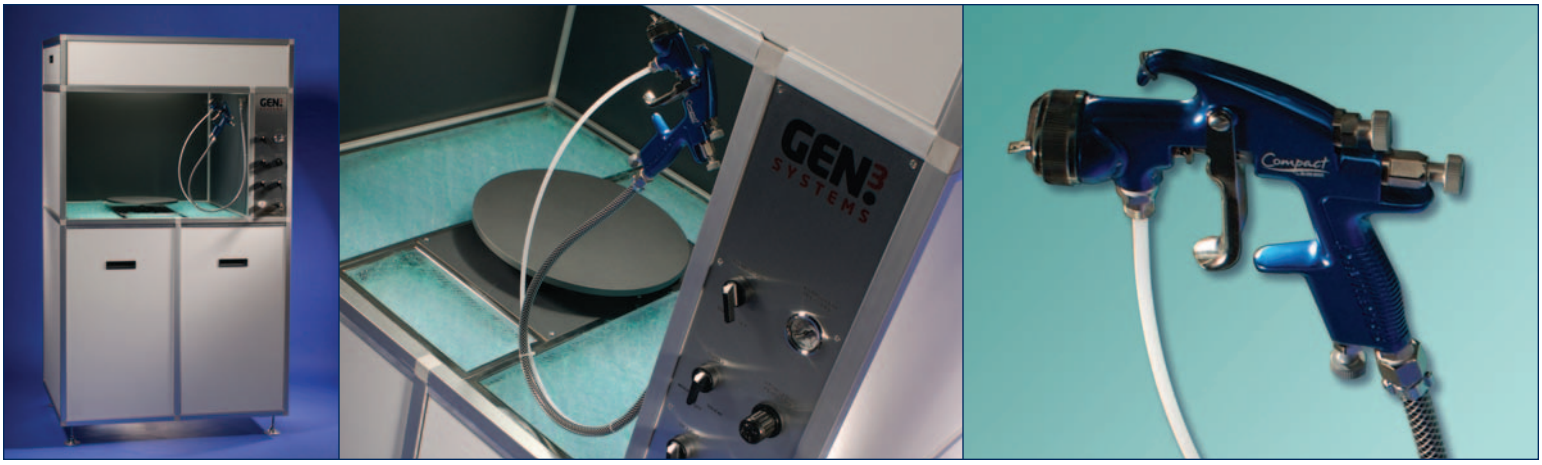

Figure 3-1: A Gen3 Systems handheld spray booth located at the EMPF.

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Tech Tips: Conformal Coating Inspection

In the field of electronics manufacturing, the end use of the product will always dictate the processes, procedures, and methods, not only for building the product, but also for testing, cleaning, and protecting the assembly in order to assure the level of quality required for proper operation. The need to protect an electronic assembly from it's end use environment may stem from any one of a number of hazardous (or potentially hazardous) conditions. Choosing the type of protective material is dependent upon matching that material's characteristics with the conditions to be overcome. Naturally, the use of a protective (conformal) coating will require some method of verification to ensure the desired level and type of protection is achieved.

There are a variety of reference documents providing specifications for conformal coatings. The intent of this article is to give an overview of inspection methods and considerations when using such coatings in the course of manufacturing an electrical or electronic product.

The five general categories of conformal coatings are:

- Type AR-Acrylic Resin
- Type ER-Epoxy Resin
- Type SR-Silicone Resin
- Type UR-Polyurethane Resin
- Type XY-Paraxylylene (also referred to as Parylene)

When establishing manufacturing processes which includes the application of a conformal coating, it is recommended that the coating be qualified in regards to physical characteristics including (but not limited to), shelf life, cure time, viscosity, fungus resistance, flexibility, flammability, dielectric withstanding voltage, and thermal shock.[1] (Note: for details on verification methods of the above characteristics consult IPC-TM-650, ASTM D-1084, and UL 94 HB.)

Once the type of coating has been established, qualified, and incorporated into a process, it is necessary to continually verify quality conformance. It is important to check the material for physical appearance, fluorescence, thickness, and full cure.

The IPC J-STD-001D specifies that conformal coatings must be fully cured and homogeneous. Also, because the intent of conformal coating is to provide an immediate barrier to a harsh environment, the standard specifies that conformal coating must be free of blisters, breaks, cracks, voids bubbles, mealing, peeling, wrinkles, or foreign material which would expose conductive surfaces to the environment.[2] Physical appearance can be easily verified by visual inspection. Magnification may be used up to 4X.

When conformal coatings contain a UV tracer (dye), inspection can be performed using an ultraviolet (UV) light source (Figure 4-1). This becomes a valuable tool for verifying complete coverage and any specified areas that should be free of conformal coating (such as electrical contacts).

The specifications for thickness of a conformal coating vary depending upon the type of coating used. The J-STD-001D specifies 0.03-0.13 mm for types AR, ER, and UR, but requires a thicker coverage of 0.05-0.21 mm for SR types. Because it is the most resilient, Paraxylylene is only required to have a thickness of 0.01-0.05 mm.[3]

The thickness of the coating can be measured in a number of ways, but most of the methods used fall into one of two general categories.

1. Dry film method: Measurement using a micrometer (or indicator accurate to 12.5±2.5µm)[4], made on a test coupon of the same type of material as the printed board or may be of a nonporous material such as metal or glass. Such measurements are to be made on a flat, unencumbered, fully cured surface of the printed circuit assembly or a test coupon.[5]

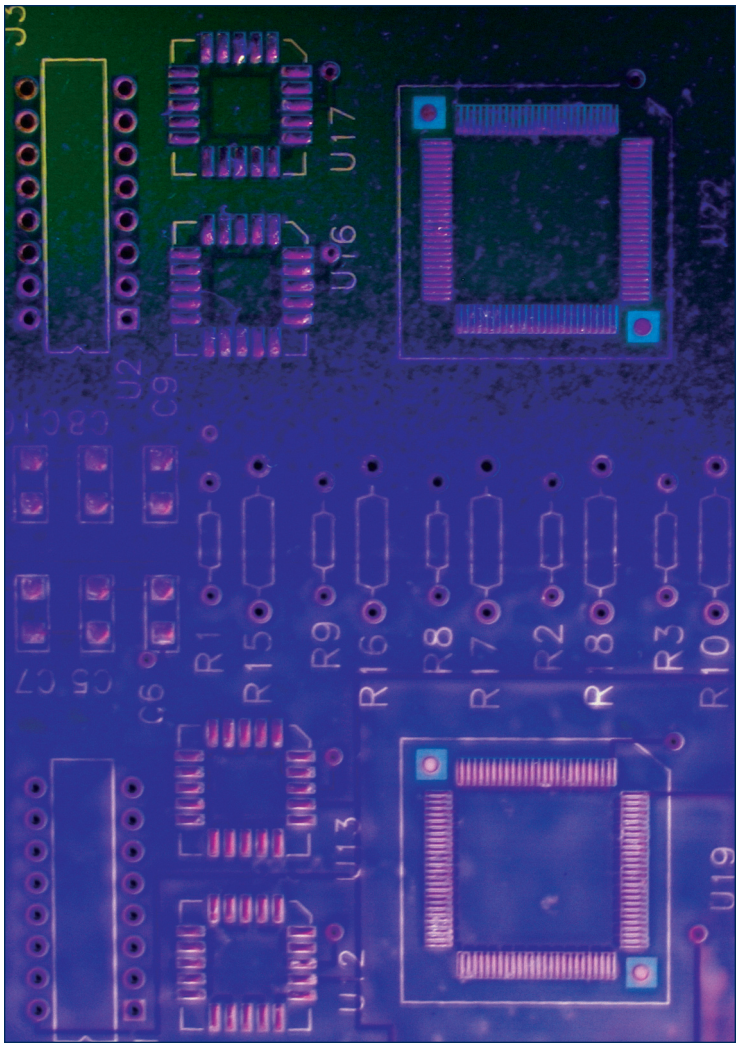

Figure 4-1: Image of a board under UV illumination with conformal coating only on the lower portion (purple area).

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Manufacturer's Corner: Easy Braid

The VPI-1000 Series Optical Inspection Systems by Easy Braid (Figure 5-1) change the way technicians "see" array packages. The unit allows the operator or technician to check every solder ball, every joint, and verify that the attachment has been performed to the specification. The endoscope enables the operator to view the object tighter, closer, and lower than other optical inspection systems currently available.

Unique to the system is Easy Braid's advanced endoscopic lens. The lens is capable of rotating 90° left/right and has a 5° angle of swing up/down. With the VPI-1000, operators can inspect under array packages with standoff heights as low as 0.002" and with clearances of just 0.043" between components. The lens design uses 2/3 fewer optical elements than other vision systems. As a result, much sharper and clearer direct images are relayed to the system's high resolution CCD camera as compared to the "shadowy" images relayed by other vision systems.

Figure 5-1: The VPI-1000 Optical Inspection System

The Easy Braid optical design shows the subject imagery in vibrant detail. While conventional designs relay an internal image repeated throughout the length of the endoscope, Easy Braid's lens has only one image – the image in front of the eyepiece. By turning the adjustment ring, the operator can easily check for bridging, cold solder joints, shorts, and other process-related failures that some inspection systems, including X-ray, may not see.

A powerful white halide light floods the underside of the component with a brightness that replicates natural daylight, maximizing the amount of visual information that can be gathered. Using a compact, high-resolution CCD camera linked to a superior flat screen LCD display, the VPI-1000 creates an image of tremendous clarity and sharpness. Images are displayed in real-time, allowing quick and easy inspection to verify the soldering process, confirm quality assurance, and identify and correct process defects. Images can also be captured and stored for future reference or reports.

The software package includes precise measurement and analysis tools, multi-focusing and image enhancement capabilities, defect diagnostics, an exhaustive defects library, preset calibrations and an easy-to-use CD manual. Operators have the data available to measure, record, annotate, analyze, and communicate component information.

The VPI-1000 is a very flexible and versatile optical inspection unit for examining component BGAs and PCBs both large and small. The endoscope is one of the crucial inspection tools for the EMPF.

For more information related to this article or to schedule a demonstration of the VPI-1000 endoscope, contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.

Ken Friedman | EAB Coordinator

The EMPF's electronic manufacturing training courses are structured to include students from a wide range of disciplines, such as Program Management, R&D, Engineering, Quality, and Operations personnel. The course content is geared specifically to meet the many challenges of the ever-changing world of electronics technology. The modular system also gives us the advantage of choosing and adding course content based on the need and skill set of the students. The customizable courses – offered at the EMPF or at the customer's site – are instructed by top-level personnel with extensive experience in their fields. They are knowledgeable in both the theoretical and practical applications of their trade. Additionally, those training at the EMPF will benefit from the hands-on experience of working in the state-of-the-art facility.

The EMPF has always been in the forefront of instructing IPC and engineering courses to the electronics industry for both the Department of Defense and industry related ventures. Our continued success depends on our ability to adapt and offer solutions to training that will benefit our partners. A perfect example of this is the training program initiated in cooperation with the Army's Communication Electronic Research Development and Engineering Center (CERDEC). This course is intended to train government personnel in the manufacturing of electronics, at various skill levels, and across various government positions. This same concept has been transitioned into our extensive curriculum of training classes.

Engineering training consists of three levels:

Level I Engineering Training

This level is focused on an intensive one-week experience for beginning to mid level engineers and technologists. The five-day sessions are conducted at the EMPF's facility, where the students begin with design concepts and end with a good hands-on experience on the manufacturing of electronic assemblies. Some of the many topics that are covered include:

- Manufacturing and documentation review
- Computer-aided design files
- Review of various design techniques
- Reviewing manufacturing bill of materials
- Review standards and specifications
- Validation of revision compliance
- Understanding product requirements
- Fundamentals of surface mount technology (SMT) and mixed technology manufacturing (Figure 6-1)

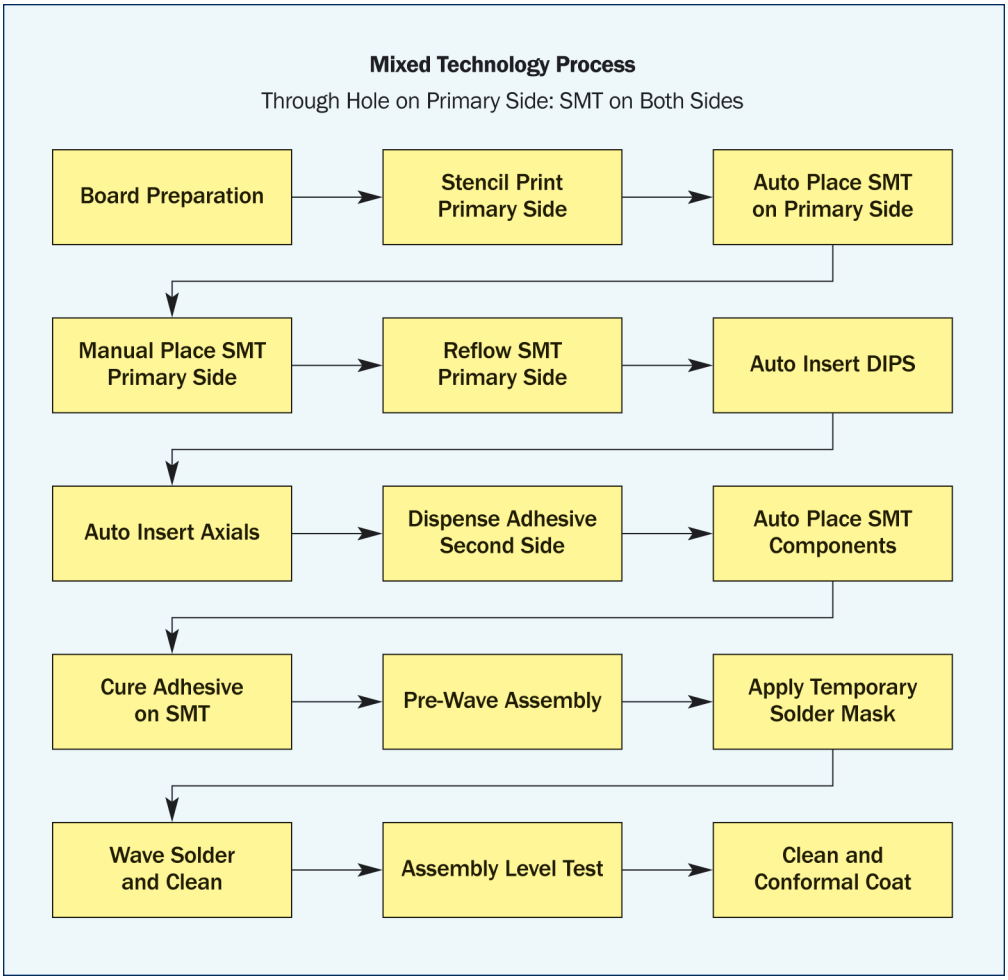

Figure 6-1: SMT Process Flow Chart

Additionally, the student builds his own take home assembly using the manufacturing methods and equipment employed in SMT, and Plated Through-Hole processes.

Level II Journeymen Course

Level II is a comprehensive program designed to educate participants on the many different processes and materials used in through-hole and surface mount technologies. The course is designed to give an overview of the critical engineering skills, requirements, and technical attributes needed for working level engineers, while acquiring the necessary training for proper facilitation of an electronic manufacturing operation. The student also gains an understanding of the skill sets pertinent to the defense acquisition process. It is an intensive program that provides students with the opportunity to learn and understand the process, tools, and materials used to manufacture electronic assemblies. It includes topics such as Design for Manufacturing, Lead Free, Design of Experimentation and Statistical Process Controls (Figure 6-2) for Electronics, Chip Scale and Ball Grid Array Technology, and other leading edge electronic manufacturing .

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Properties of Low Dielectric Constant Laminates

(continued from page 1)

The RT/duroid 5880LZ laminate has several other benefits to offer. Besides a very low Dk of 1.96 and a Df of 0.0019, special filler technology makes the CTE of this material approximately 42 ppm/ºC for all three axes.

A comparison of different laminates used in the high frequency industry are shown in Figure 1-1.

A topic that is often overlooked is the TCDk of the substrate. The thermal coefficient of dielectric constant is a property which is inherent in all PCB materials. Many times this property is not well considered in the design phase, which can be adversely realized in the end-user phase of a project. The changes in dielectric constant with temperature can be very significant for many high frequency materials. Most PTFE materials have a relatively high TCDk, or in other words, the dielectric constant will change more with a change in temperature. In some applications this will be more obvious than others. Many typical PTFE substrates will have a TCDk which is 150 ppm/ºC or greater. The RT/duroid 5870 and 5880 are lower than this value; however the 5880LZ substrate has a very good TCDk of 22 ppm/ºC. Basically, when the 5880LZ material is used in an application where the PCB can be exposed to a wide range of temperatures, the dielectric constant will remain much more stable than nearly all PCB laminates. Of course a stable dielectric constant across a range of temperatures will yield stable circuit impedance and a much more stable system performance. A comparison of the TCDk for the 5880LZ laminate and a woven glass PTFE substrate is shown in Figure 1-2.

The control of the Dk value as the material is manufactured is critical, so the end user will have consistent electrical performance. The RT/duroid 5870 and 5880 have their Dk values held to a tolerance of ± 0.02 and the RT/duroid 5880LZ is ± 0.04 as reported by the industry standard IPC test method IPC-TM-650 2.5.5.5c.

The density of RT/duroid 5880LZ is significantly less than any traditional high frequency laminate, which translates to a much lighter PCB. The density of most PTFE substrates is about 2.20 gm/cm^3 while the 5880LZ laminate is 1.37 gm/cm^3. This considerable reduction in density will yield much lower payload or airborne weight as it relates to the high frequency PCB. This is a great benefit for airborne or space deployed applications.

There are several PCB manufacturing issues for any laminate and PTFE laminates are no exception. Since these laminates have been in use for many years, the fabrication issues are well understood. The main issues for circuit fabrication are: drilling, plated through hole (PTH) preparation and plating, softness of the material, and dimensional stability. Very specific PCB fabrication guidelines for RT/duroid materials are provided on the Rogers Corporation website.[1] In general, to address these issues:

1. The main consideration for hole drilling is to minimize heating the substrate to prevent smear.
2. To allow the liquid processing that will deposit copper on the wall of the drill hole for PTH, the PTFE material must be made wettable by removing a fluorine molecule. The removal can be done by a wet process using sodium naphthalene or by a special plasma process. For a nearly pure PTFE substrate, the wet process will generally have better results.

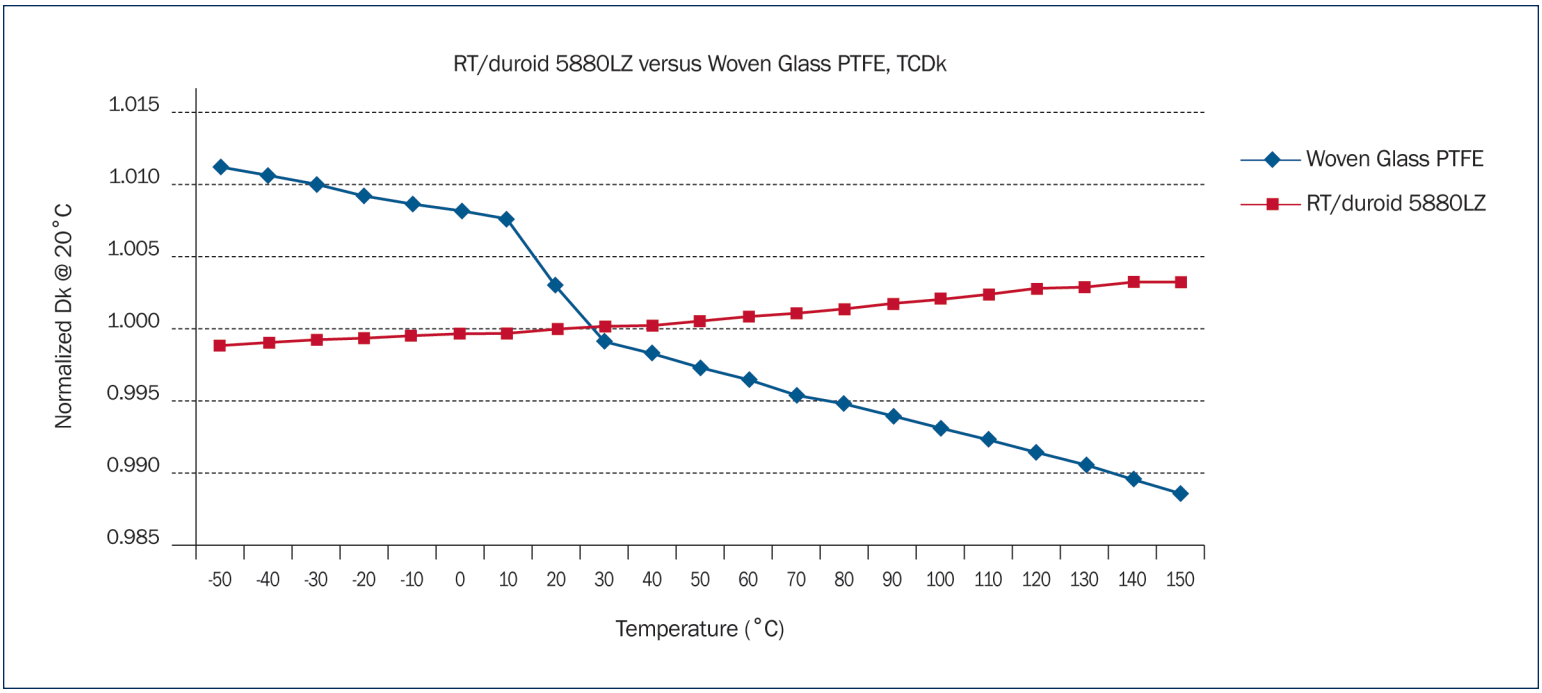

Figure 1-2: PTCDk comparison between a woven glass PTFE laminate and RT/duroid 5880LZ.

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Properties of Low Dielectric Constant Laminates

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3. The softness of the material will translate into process handling and sometimes dimensional stability issues. This material should not be scrubbed or mechanically stressed during the PCB fabrication process.

The RT/duroid family of products offers several laminates with a low Dk. The RT/duroid 5000 family of products has the lowest Dk values on the market today as well as stringent control of this property. The CTE issue associated with PTFE based laminates can be overcome by the use of a thinner laminate and multilayers using hybrid constructions. Also, with the introduction of the 5880LZ laminate, the CTE is in the range where high reliability for PTH is expected. The TCDk issue is sometimes overlooked and can be an issue for some laminates and applications. The 5880LZ has a very low TCDk, enabling it to be used in temperature varying applications predictably. Lastly, the low density of the 5880LZ can be very beneficial to applications where weight is restricted.

Rogers Corporation is a circuit materials supplier for the high frequency PCB industry. With an extensive line of products, the RT/duroid® product line has been used in a wide-range of applications for many decades. Of these products, the RT/duroid 5000 family of high performance laminates offers low Dk laminates with very low Df. A recent addition, RT/duroid 5880LZ laminate, has the lowest Dk and offers several improvements to most other PTFE laminates.

For more information about these or other high-frequency laminates suitable for your design, contact Mr. John Coonrod with Rogers Corporation, at 480.961.8398, or via email at john.coonrod@rogerscorp.com.

[1] *RT/duroid® 5870/5880/5880LZ High Frequency Laminates*. Rogers Corporation, 2009. Web. 27 Jan. 2010. <http://www.rogerscorp.com/acm/products/10/TR-duroid-5870-5880-5880LZ-High-Frequency-Laminates.aspx>.

ROGERS CORPORATION

Ask the EMPF Helpline!

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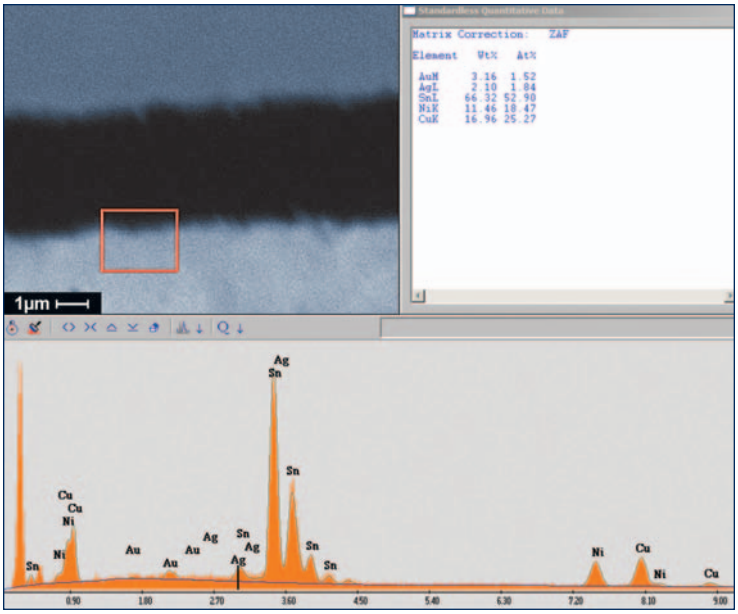

Figure 2-3: SEM-EDS data for the solder ball side of an outer solder joint that cracked.

Optical microscopy, X-ray fluorescence (XRF) spectroscopy, and/or SEM-EDS techniques were recommended to determine the plating thickness and porosity. The customer was able to provide a bare board from a similar lot to the previously examined assembly. Figure 2-4 shows the uneven and apparently porous gold surface of a representative BGA pad location. Figure 2-5 shows the SEM-EDS elemental mapping for a BGA pad where nickel appears to be visible through thin patches of the gold plating.

Optical microscopy showed uneven gold plating on the pads throughout the board. The SEM-EDS data also showed patchy gold plating with nickel apparently being exposed through the gold. All of this data indicates that the process producing these boards was not properly controlled.

The EMPF recommended that the customer speak with their bare board manufacturer about improving the hard gold over hard nickel plating process or switching to other surface finishes, such as soft gold over nickel plating, electroless nickel immersion gold (ENIG), or immersion silver (IAg).

The customer made a new set of boards with an IAg surface finish and provided them to the EMPF in the bare board and finished assembly states. Figure 2-6 shows images of a representative solder joint in which good bonding along the board pad to solder ball interface was observed.

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Ask the EMPF Helpline!

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The EMPF recommended that the customer perform incoming quality acceptance inspections on PCBs as part of their supplier quality control strategy until such time that the supplier has proved capable of providing material acceptable to the appropriate requirements. The acceptance testing should include solderability testing, non-destructive plating thickness measurement, and visual workmanship assessment to ensure compliance to the requirements of IPC-6012 - Qualification and Performance Specification for Rigid Printed Boards and IPC-A-600 - Acceptability of Printed Boards. Failure to meet these requirements should be used as justification to reject individual PCBs and/or entire board lots, as necessary.

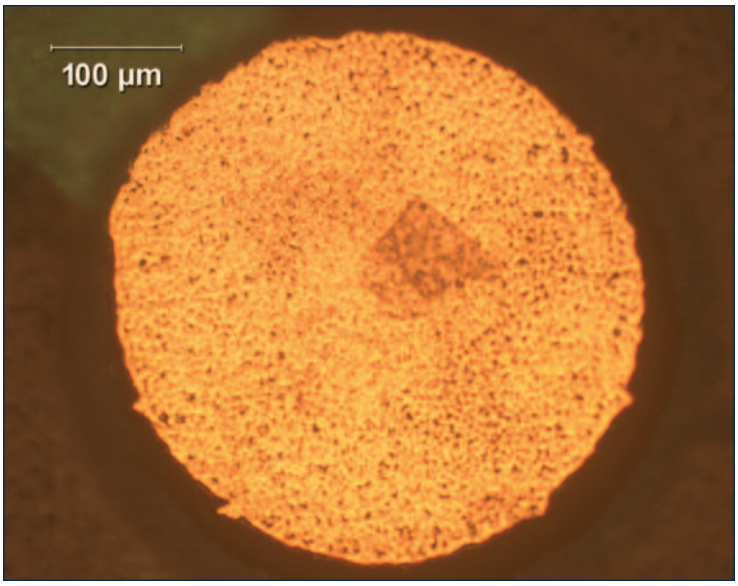

Figure 2-4: Optical image of the rough surface of a pad.

Additionally, the supplier should also perform inspections to ensure that nonconforming material is not provided to customer. The customer's drawings should place requirements on their supplier(s) by providing notes that use language similar to the following:

- Manufacture in conformance with the requirements of IPC-6012 (latest revision), Class [1, 2, or 3, as appropriate].
- Inspect per the requirements of IPC-A-600 (latest revision), Class [1, 2, or 3, as appropriate].

The EMPF can provide board and assembly qualifications, and inspections, as well as failure analysis to determine the root cause of solder joint failures. The EMPF can further assist with surface finish analysis, cleaning processes and cleanliness testing for ionic and organic residues, and engineering services. Ion chromatography, bulk ionics (Ionograph) testing, attenuated total reflectance Fourier transform infrared (ATR-FTIR) spectroscopy, X-ray fluorescence (XRF) spectroscopy, and ultraviolet/visible (UV-Vis) spectroscopy, optical microscopy, and scanning electron microscopy with energy dispersive X-ray spectroscopy (SEM/EDS) capabilities are all on hand to aid in the determination of possible contamination issues and their root causes. Contact Ken Friedman, at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org for more information.

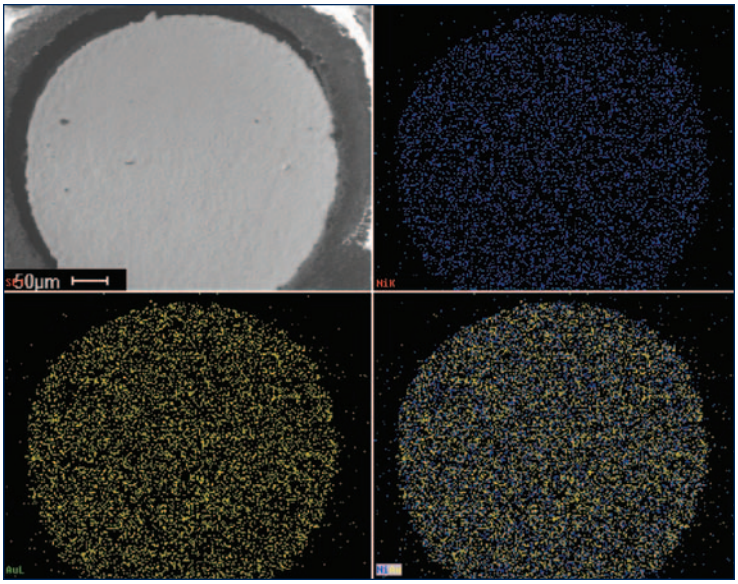

Figure 2-5: SEM-EDS elemental map of a pad. [Top left - image, top right - nickel (blue), bottom left - gold (yellow), bottom right - overlay of both.] The overlay map shows patches where the nickel may be exposed through the gold.

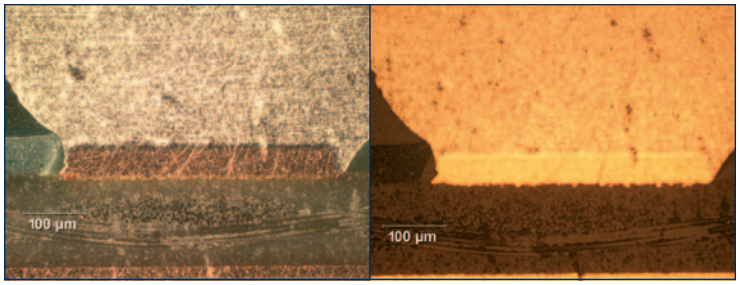

Figure 2-6: Optical image of a good solder joint along the board pad to solder ball interface. [Dark field image on left, bright field image on right.]

Sean Clancy, Ph.D. | Research Associate/Chemist

Conformal Coating Processes

(continued from page 3)

The final coating process available at the EMPF is selective spray coating. This process has recently been introduced to the Demonstration Factory and should provide the advantages of automating the spray coating process (low process variability, high throughput) without some of the disadvantages of manual spray coating (labor intensive masking or costly hard-tooled fixtures). The major disadvantage of automated spray coating is the initial programming required for each application. Once the programming task is completed, the automated process is well suited for high volume applications regardless of product mix as well as applications where masking isn't a viable option.

If you are in need to assistance with your conformal coating application process, contact the EMPF at 610.362.1200 or www.empf.org.

[1] Fullerton, Jason. "Tech Tips: Coating Application Methods." *Empfasis* (May 2009). ACI Technologies Inc., May 2009. Web. <http://www.empf.org/empfasis/2009/May09/tech_tips_509.html>.

Jason Fullerton | Sr. Product and Applications Engineer

Tech Tips: Conformal Coating Inspection

(continued from page 4)

2. Wet film method: This alternative method measures the coating while it is still wet (before curing has been completed) and provides for calculations that will indicate the thickness after curing has been completed. This method is preferred when a dry film method is not practical or would be destructive.

For more details on methods and processes regarding the application and measurement of conformal coatings, the EMPF offers the IPC J-STD-001D course, as well as the IPC 7711/7721 Rework and Repair course. Please contact the Registrar at 610.362.1295 or visit our website at www.aciusa.org/courses.

[1] *Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies*. IPC-CC-830B. Association Connecting Electronics Industries. Table 3-1.

[2] *Requirements for Soldered Electrical and Electronic Assemblies*. ANSI/IPC J-STD-001D. Association Connecting Electronics Industries. Clause 10.1.2.2.

[3] Ibid. Clause 10.1.2.1.

[4] IPC-CC-830B. op.cit. Clause 4.7.4.

[5] ANSI/IPC J-STD-001D. op.cit. Clause 10.1.2.1.

Ross Dillman | Technician/Instructor

Upcoming Courses

IPC J-STD-001

Certification: March 15-19 | *Recertification:* April 14-15

This course provides an in-depth study and hands-on application of the national standard for soldering as well as all materials necessary to conduct operator training.

IPC A-610

Certification: April 19-22 | *Recertification:* May 24-25

Achieve the highest quality and most cost-effective productivity by knowing how to correctly apply the IPC A-610 acceptability criteria.

CONTACT THE REGISTRAR via phone at **610.362.1295**, email at **registrar@empf.org** or online at **www.aciusa.org/courses**

(continued from page 6)

Level III Managers Course

This is a one-day course developed to provide training for senior level engineers and managers. It provides an overview that will identify the key functional and physical characteristics critical to the infrastructure of an electronic assembly and manufacturing plant. The course covers the three main sections dealing with material management, new technologies (Figure 6-3), and critical legislation. The course design helps the individual clarify the significance of implementing controls in various areas such as configuration management, sustainment of product, control change, documentation, prohibitive material process, and the effects of commercial off the shelf (COTS) products on the material infrastructure.

The multi-level engineering program was a response to a need that helped our partners maintain the necessary skilled personnel to produce effective quality products. The EMPF has worked diligently to maintain its training expertise on behalf of our valued customers to make your training needs more affordable and effective.

Should you have any questions please contact the Registrar at 610.362.1295 or visit our website at www.aciusa.org/courses.

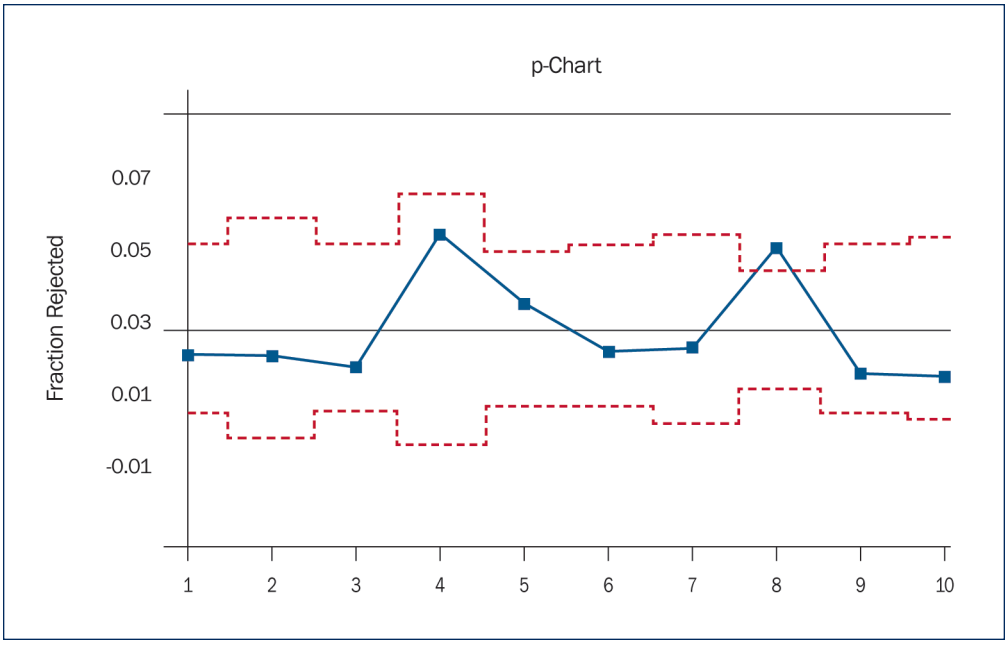

Figure 6-2: SPC p-Chart

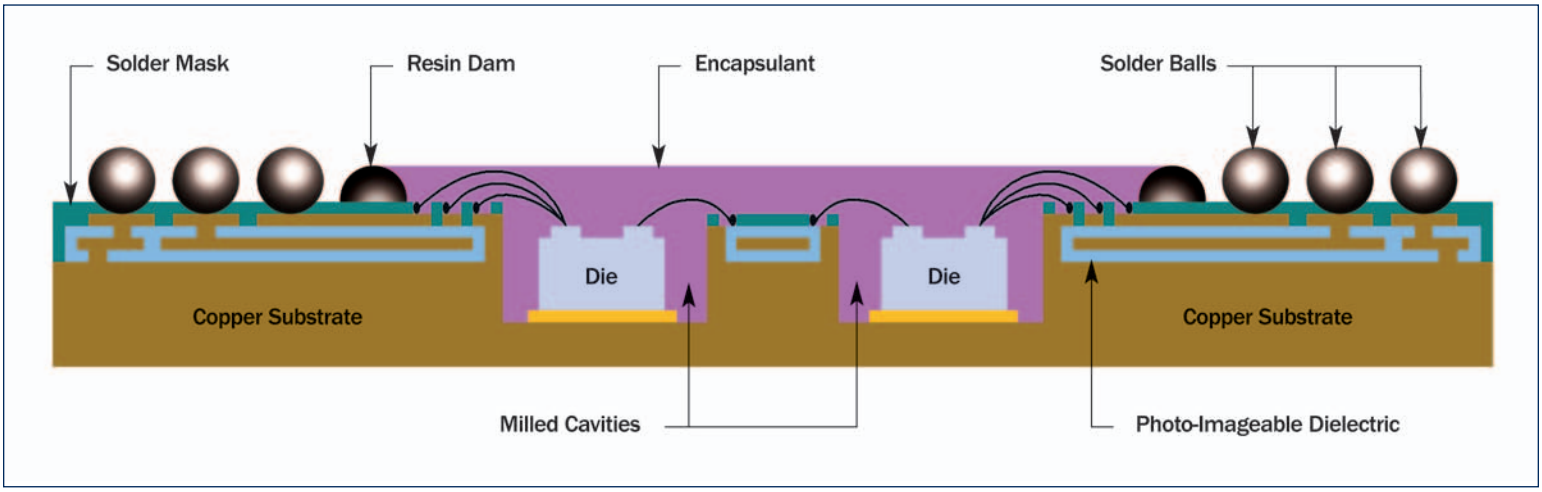

Figure 6-3: Nano Technology

Carmine Meola | R&D Projects Manager

ACI Technologies, Inc.

2010 Class Schedule

National Electronics Manufacturing Technology Center of Excellence

Electronics Manufacturing

Boot Camp A
March 1-5
May 3-7
September 13-17
November 1-5

Boot Camp B
March 8-12
May 10-14
September 20-24
November 8-12

CIS/Operator

IPC J-STD-001
Call for Availability

IPC A-610
Call for Availability

IPC 7711/7721
Call for Availability

IPC/WHMA-A-620A
CIS Certification
February 16-18
April 19-21
June 28-30
September 27-29
December 20-22

High Reliability Addendum

IPC J-STD-001 DS
CIT Certification
January 15
February 26
April 16
May 28
August 27
October 8

IPC CIT Challenge Test

January 29
February 19
April 23
June 18
July 16
August 20
October 15
November 19
December 17
Call for Additional Availabilities

IPC Certifications CIT/Instructor

IPC J-STD-001
CIT Certification
January 4-8
February 1-5
March 15-19
April 26-30
June 7-11
July 19-23
August 30 - September 3
October 18-22
December 6-10

IPC J-STD-001
CIT Recertification
January 13-14
February 24-25
April 14-15
May 26-27
July 14-15
August 25-26
October 6-7
November 17-18
December 15-16

IPC A-610
CIT Certification
January 4-7
February 8-11
April 19-22
June 14-17
August 16-19
October 11-14
December 6-9

IPC A-610
CIT Recertification
January 11-12
February 22-23
April 12-13
May 24-25
July 12-13
August 23-24
October 4-5
November 15-16
December 13-14

IPC A-600
CIT Certification
January 26-28
March 22-24
June 21-23
September 7-9
November 29 - December 1

IPC 7711/7721
CIT Certification
January 25-29
March 22-26
July 26-30
October 25-29

IPC 7711/7721
CIT Recertification
March 8-9
May 17-18
June 14-15
September 13-14

Skills

BGA Manufacturing, Inspection, Rework
January 19-20
April 5-6
June 28-29
October 11-12

Chip Scale Manufacturing
February 16-18
May 26-28
August 11-13
December 13-15

Continuing Professional Advancement in Electronics Manufacturing

Design for Manufacturability
February 8-9
May 24-25
August 9-10
November 22-23

Failure Analysis and Reliability Testing
March 15-17
May 17-19
September 27-29
November 15-17

Lead Free Manufacturing
February 22-23
June 7-8
October 4-5
December 20-21

Contact the Registrar for course information and pricing: *phone:* 610.362.1295 *email:* registrar@empf.org

Electronics manufacturing assistance is available via the EMPF Helpline: *phone:* 610.362.1320 *email:* helpline@empf.org

Custom courses and on-site training are available. ACI is conveniently located next to the Philadelphia International Airport.

IPC® Training Center

All courses and dates subject to change without notice.

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