

#### A publication of the National Electronics Manufacturing Center of Excellence



#### ISO 9001-2000 Certified

Michael D. Frederickson, EMPF Director

Barry Thaler, Ph.D. • bthaler@aciusa.org EMPF Technical Director *Empfasis* Technical Editor

> Paul Bratt • pbratt@aciusa.org Empfasis Editor

#### In this Issue

COTS Cooling1
Ask the EMPF Helpline!2
Non-Destructive Test Methods
Tech Tips: BGA Reballing4
Manufacturer's Corner: Metcal5
Failure Analysis Training Course6
Training Center Course Schedule12



ACI Technologies, Inc. One International Plaza, Suite 600 Philadelphia, PA 19113 610.362.1200 • fax: 610.362.1290 Helpline: 610.362.1320 web: www.empf.org • www.aciusa.org



Industrial Advisory Board

Gerald R. Aschoff, The Boeing Company Jack R. Harris, Rockwell Collins Richard Kidwell, ITT Industries, Avionics Division Gary Kirchner, Honeywell Dennis M. Kox, Raytheon Gregory X. Krieger, BAE Systems Edward A. Morris, Lockheed Martin Andrew Paradise, Northrop Grumman

### **COTS** Cooling

The EMPF is currently working on a project where one of the challenges is removing a large quantity of heat from audio amplifier circuits. This challenge is further complicated in that the heat generating circuits are located in a rack mounted box that needs to be shielded from electro-magnetic interference (EMI). Mechanically, this means that there cannot be open passages into the rack mounted box. We will first review the basic types of cooling available as commercial off-the-shelf (COTS) systems for the electronics industry, then discuss the pros and cons of each for different applications, and finally reveal the criteria and solution for the EMPF project.

When working with circuitry and components requiring cooling in general, there are several options available for the dispersion of heat. Heat sinks, liquid cold plates, heat pipes, and thermoelectrics were trade studied within this project. Heat sinks are simply thermally conductive (typically aluminum) masses attached to heat generating electronic devices. The heat sink can be as basic as a block or it can be machined with fins to increase the surface area in contact with the surrounding air. Heat sinks can use natural convection or forced convection for cooling. Natural convection relies on the natural tendency for warm air to rise away from the heat sink to keep a constant stream of cool air crossing the unit. Forced convection employs the use of a fan to actively move air across the heat sink for cooling. Natural convection is a simpler solution that requires no moving parts, so it is typically the preferred method of cooling. A major drawback to natural convection is that a device or assembly that generates a large amount of heat generally requires a large heat sink. If the design constraints of the product require a small overall package, a cooling fan will more than likely be required. The example in Figure 1-1 shows a forced convection heat sink with a fan blowing air between the fins for added cooling capacity.

Most electronic devices that convert power have at least one heat sink on them. The examples in Figure 1-2 show transistors connected to solid heat sinks. The unit on the left uses the aluminum plate in room temperature (25°C) air to dissipate the added heat. The unit on the right relies on connections to exterior aluminum plates to provide a thermal conduction path at temperatures close to 50°C. As a component generates more heat and the size of the heat sink cannot be increased, fins can be added to increase the surface area in contact with its surroundings.

Liquid cold plates are again thermally conductive masses, but they have passages that allow a coolant fluid to be pumped through them. Liquid cold plates allow the transfer of heat to a more remote



Figure 1-1: A forced convection heat sink with a fan blowing air between the fins for added cooling capacity.





## Ask the EMPF Helpline!

Improving Post-Rework Flux Cleaning for Improved Reliability

A customer called the EMPF Helpline and asked for assistance in evaluating their rework process for a new Class 1 assembly process which failed reliability testing.

In this case, visual inspection revealed the issue to be excessive flux residue remaining around the reworked solder joints, most likely due to improper cleaning after rework. Properly cleaning an assembly after rework is extremely important in maintaining board reliability. Ionic contamination left by flux residues can lead to corrosion and dendrite growth, two common causes of electronic shorts and opens. Identifying and implementing a cleaning solution for this assembly was necessary to greatly improve the reliability of the assembly. The EMPF offers various



Figure 2-1: Acceptable Flux Residue

analytical techniques (ROSE, IC, FT-IR, SIR) to determine the root cause of contaminant problems, and to evaluate the effects of process or materials changes on cleanliness.

Figure 2-1 shows an example of a solder joint with acceptable flux residue per IPC-A-610D Acceptability of Electronic Assemblies guideline. The joint is clean, with little or no evidence of solder residue. On the contrary, it is easily seen in Figure 2-2 that a large area surrounding the solder joint is covered in flux residue. This solder joint clearly was not cleaned properly. According to the Joint Industry Standard requirements, IPC J-STD-001D, the maximum rosin flux residue levels for process compliance are as follows:

Class 1 assemblies less than 200 micrograms / cm<sup>2</sup>

Class 2 assemblies less than 100 micrograms / cm<sup>2</sup>

Class 3 assemblies less than 40 micrograms / cm<sup>2</sup>

The recommended RMA flux removal method requires a saponifier heated from 100 to 150°F to properly remove any residues. Deionized water is recommended for the final rinse. Reagent grade isopropyl alcohol (IPA) can also be used for manual cleaning by agitating with an acid brush. The affected board was cleaned using these methods and retested to verify Class 1 compliance. The more extensive cleaning process was proposed for implementation at the customer site in order to improve future reliability testing results.



Figure 2-2: Unacceptable Flux Residue

The EMPF has the equipment and the experience to assist with our customer's process development needs. For customers interested in learning more about flux selection and choosing the right cleaning process for performance and cost effectiveness, we recommend participation in the EMPF's Electronics Manufacturing Boot Camp and IPC certification classes. Students of these courses gain an understanding of the concerns about cleanliness and residues common with electronic devices, the types of residues that are considered benign or harmful, the various cleaning chemistries and processes, safety issues, and the most commonly used cleaning equipment.

For more information please contact the registrar at 610.362.1295, via email at registrar@empf.org, or find course descriptions on the web at http://www.aciusa.org/courses.



Dan Perez R&D Engineer





**F** ailure analysis (FA), by its very nature, is needed only when things go awry. Before any testing is performed on the sample, a decision must be made as to whether or not the sample is allowed to be destroyed in the process of testing. Non-destructive testing can allow for re-use of the assembly since the functionality is not altered, but there still remains the possibility that inadvertent damage can occur through the course of the analysis. If non-destructive testing is preferred, then the following types of analysis can be performed. The testing can be divided into four categories: visual, X-ray (X-ray imaging and X-ray fluorescence), cleanliness (resistivity of solvent extract, ion chromatography, and Fourier transform infrared spectroscopy), and mechanical (non-destructive wire bond pull).

#### **Visual Examination**

#### Optical Microscopy with Digital Imaging

Optical microscopy and photography provide a permanent visual record of the sample, from the point of arrival to the laboratory through each step along the way in the determination of the root cause of the failure. A stereo microscope is used in optical microscopy to give good depth of field when the sample is placed directly underneath the main lens. When used with calibration grids and the appropriate software, images can be captured with scale bars and measurements of features, at magnifications ranging from 7x to 90x.

Figure 3-1 shows a case where salt was deposited on an unprotected portion of an assembly and with the addition of high humidity and electrical bias; a dendrite grew between two adjacent conductors and caused an electrical short. This failure was due to exposure to a corrosive environment without adequate conformal coating protection.

Figure 3-2 shows a partial fingerprint on the assembly, underneath the conformal coating. The oils from the finger print contributed to the poor adhesion of the coating, which in turn led to the dendrite seen in Figure 3-1.



Figure 3-1: Image of a dendrite growing between two pins causing a short.



Figure 3-2: The oils from this fingerprint contributed to poor adhesion of the conformal coating and led to the corrosion seen in Figure 3-1.

#### **Optical Inspection System**

An optical inspection system is similar to optical microscopy except the lens is placed very close to the board, nearly touching it, and a mirror directs the light path 90°, so that features to the right (or left) of the lens can be viewed. Fine features underneath components can be observed, especially the first two to five rows of a ball grid array (BGA) component. The row depth is dependent on the lighting and space beneath the component. The goal is to see if the solder balls have collapsed properly after undergoing the reflow process and if any abnormalities exist, such as contamination or materials bridging leads.

Figure 3-3 shows a slight misalignment of a row of solder balls. This is acceptable per IPC-A-610 Rev D since the BGA solder balls did not violate the minimum electrical clearance. However, it is a process indicator of a potential issue in the manufacturing process due to either manual placement of the BGA or an alignment issue in the pick-and-place system.



Figure 3-3: Image of a slight misalignment of a row of solder balls. This is a process indicator that either the manual placement or the pick-and-place system was slightly off.







## Tech Tips: BGA Reballing

In the current economic environment, the ability to reuse ball grid array (BGA) components that have failed due to solder defects may be an efficient way for electronics manufacturers to reduce costs. Cost may not be the only driving factor in the decision to engage in this recycling practice. The increasing demands placed upon the complexity of microprocessors and integrated circuits (ICs) has decreased the availability of some components, and increased their lead time. Because of this, reballing may provide a means to meet schedule, reduce rework turn-around time, and give a manufacturer a decisive advantage over other companies in an ever increasingly competitive market. This article will discuss the process of reballing BGA components, examining preparation (the preform method, the screen method), and cleaning and bake-out.

Before attempting to reball a BGA, consider the solder alloy. Lead-free components require a different reflow profile from those using a tin/ lead alloy. Also consult the manufacturer's data sheet for precautions regarding component moisture sensitivity and limitations on the number of reflows cycles the component can tolerate. Repeated reflow cycles may void a component's warranty.

#### Preparation

The first step in reballing a BGA is to remove the old solder from the component lands. The use of a wide blade soldering iron tip works best. With the application of flux and solder braid, the wide blade tip can be drawn across the component surface allowing the residual solder to be wicked off of the component lands and into the solder braid. Care must be taken to avoid downward pressure on the component for fear of damaging the lands. After the excess solder has been removed, clean off any remaining flux residue using a solvent that is chemically matched to the type of flux. Isopropyl alcohol (IPA) can be used with most common resin type fluxes. If an aqueous cleaning system is used in conjunction with a low residue or no-clean flux, be certain to match the soponifier with the flux chemistry.

#### **Preform Method**

One method of successful reballing is the preform method. This employs a solder preform used in conjunction with a simple frame that matches the BGA component's outside dimensions. The preform is constructed with precisely spaced solder balls sandwiched between a cardboard laminate that has been saturated with a water-soluble flux. Once the component has been properly prepared, place the preform into the frame with the ball-side facing up, apply some water-soluble flux paste to the lands of the component and then set the component into the frame on top of the preform. Now you need only reflow the frame, using convective heat to wet the solder balls to the component lands. Once the component cools, the cardboard laminate can be removed and the component cleaned using deionized water. Many electronics manufacturers have found this to be an efficient way to reclaim components that would otherwise have been discarded and the wide variety of preform shapes and sizes make this method of recycling highly effective.



Figure 4-1: BGAs

#### **Screen Method**

The screen method employs a screen stencil of non-solderable material. You begin by applying tacky (paste) flux to the properly prepared component lands. You then place the component in a specialized fixture (the fixture should match the outer dimensions of the component). Set the screen stencil over the component lands ensuring that the holes in the screen line up with the component lands. Then place individual solder balls on top of the screen and move them about so they fall into the holes of the screen which are already aligned with the lands. Take care that all holes are filled and that no excess balls can roll about within the fixture. Now simply reflow the entire fixture allowing the solder balls to wet to the component lands.

#### **Cleaning and Bake-Out**

After reballing is complete, the manner in which the component is cleaned is dependent upon the type of flux used during the process. Isopropyl alcohol may be used as a solvent with resin/rosin based flux (a test method may need to be developed to ensure no residue is left behind). When using preforms however, deionized water must be used to clean the component, because the laminate comes pre-saturated with water-soluble flux. Although the preform method is quite efficient, it requires an additional step. It is necessary to perform a bake-out cycle of the component prior to use because of possible water absorption by the component. Consult the manufacturer's data sheet for recommendations on moisture removal from BGA components.

When properly employed, the practice of reballing can save money and time for a manufacturer and therefore a thorough understanding of the benefits of this process can be a valuable investment of time and resources. For more information, please contact the EMPF helpline at 610.362.1320 or log onto the EMPF website at www.empf.org.



Ross Dillman Technician/Instructor





### **Manufacturer's Corner: Metcal**

In today's fast paced manufacturing environments, the main challenges for hand soldering and rework are driven by three factors. First, more heat is needed for lead-free solder and other thermally challenging conditions. Second, higher levels of precision are needed for increasingly smaller components. And finally, greater control is needed for components and substrates that require limited exposure to high temperatures.

The EMPF is currently using the new MX-5000 Soldering/Desoldering and Rework System by Metcal. This new offering is a system that enables increased productivity and process control for a wide range of applications. Similar to the older MX-500, the new MX-5000 increases output power, adds process feedback, and improves application flexibility with new hand-piece ergonomics.

#### **Increased Power**

With nearly double the power of the older MX-500, the MX-5000 timeto-recovery increases production rates and throughput. The challenges of high mass components, multilayered boards, and lead-free solders are seamlessly matched.

#### **Improved Ergonomics**

The MX-5000 Series offers new soldering hand-pieces which are designed for ease of use, performance, and operator comfort. The hand pieces designed to work with the MX-5000 are: the Advanced Soldering Hand-piece model #MX-H1-AV, the Ultrafine Hand-piece, the Precision Tweezers hand-piece and the Desoldering Hand-piece model #MX-DS1.

#### **Greater Process Control**

SmartHeat Technology in every MX-5000 senses the specific thermal demand directly at the solder pad and delivers the precise quantity and flow of thermal energy to ensure that soldering and rework are always performed at safe, controlled temperatures.

The new MX-5000 Series provides users with a wide range of choices to address conduction soldering and rework processes. At the core of each system is a microprocessor controlled power supply that provides more power, the highest level of precision, and advanced user features for greater process control. It has a built-in power indication meter with digital display and bar graph which provides the operator with feedback on the status of the soldering operation. Whether using a large mass rework tip for quad flat packs (QFPs) or a fine-point soldering tip, the power indication meter is a valuable resource for making consistent, acceptable solder joints.

The system has four mode indications. "Ready Mode" indicates the hand-piece is removed from the work stand and is ready for soldering or rework. "Power Mode" is when the hand-piece's tip is in contact with the load and the power indication meter provides graphical and numeric feedback on the system power output. "Sleep Mode" indicates that the hand-piece is at rest in the work stand with reduced power to the hand-piece. "Power Save" mode is a programmable feature that allows a supervisor to set the desired time to cut off power to the hand-piece.

#### **More About Comfort and Control**

The advanced soldering hand-piece is a general purpose tool for single task soldering, touch-up soldering, surface mount device (SMD) rework, and pad clean-up. This hand-piece offers a choice of three interchangeable grips to meet operator preferences for comfort and feel, resulting in higher levels of productivity.

The ultrafine hand-piece is designed for very fine soldering on mini and micro components as small as 0.2 mm.

For efficient and ergonomic removal of discreet and small outline integrated circuit (SOIC) components, the tweezer hand-piece increases productivity with greater removal speed and increased precision. The tweezers are able to rework devices as small as 0201 by combining finetip soldering cartridges and a multiple axis hand-piece adjustability to achieve proper tip alignment.



Figure 5-1: The Metcal MX-5000 Soldering/Desoldering and Rework System.

The high power desoldering hand-piece is designed for plated-throughhole component desoldering. The easy-to-grip handle allows the task to be completed quickly and comfortably. This "shop-air" hand tool, in combination with the new MX-5000 Series power supply, provides exceptional thermal performance on difficult ground planes and other high-mass applications.

As a supplement to all the refinements of the MX-5000, the new Metcal TipSaver Work stand improves tip life as well as operator ergonomics. When placed in the work stand, the "Auto-Sleep" feature reduces the power to the hand-piece which substantially decreases tip oxidation, a major cause of reduced tip life. The TipSaver Work stand is available with a soft, coiled brass tip cleaner or with both the brass cleaner and the traditional sponge holder. Many users prefer the brass-only option, as this reduces the potential to introduce contaminants to the tip, which can occur with poorly maintained sponges. The work stand also has an





### **Failure Analysis Training Course**

The EMPF training course "Failure Analysis of Electronic Assemblies" provides a general overview for investigative work on failed electronics assemblies and devices. The course spans three days and includes lecture, case study discussions, lab sessions, and demonstrations of on-site equipment and instrumentation. Students are welcome to bring samples to be analyzed during the lab and demo portions of the course. In addition, students can benefit by sharing and discussing their own failure analysis experience faced at their job. This course combines both classroom lecture material, as well as hands-on experience in the analytical wet lab and microscopy lab. Students from a wide background of both government and private industries have attended this training course. They have included quality engineers, manufacturing engineers, technicians, and managers who wanted to broaden their understanding of failure analysis and learn more about specific techniques or methodologies.

- Ion Chromatograph (IC), Ionograph, Fourier Transform Infrared Spectroscopy (FTIR), UV-Vis Spectroscopy
- X-Ray Inspection, Optical Inspection, X-Ray Fluorescence (XRF)
- Wetting Balance, Decapsulation Techniques, Sequential Electrochemical Reduction Analysis (SERA)
- Manual and Automatic Grinder/Polisher, Integrated Circuit Grinder/Polisher

Catastrophic failures from environmental testing will often be investigated by failure analysis for root cause following standards specified by ASTM, JEDEC, IPC, and MIL-STD. A tour of the EMPF facilities on the manufacturing floor will show the environmental test equipment commonly used for reliability testing.

- Salt Fog Chamber
- Steam Ager



Figure 6-1: Images from a scanning electron microscope can reveal the cause of a failure. In this case, solder fracture between the pin and the plate through hole is clearly seen.

The following topics will be covered in the morning lectures:

- Failure Analysis Methodology
- Bare Board Defects
- Failure Modes of Advanced Packages
- Component Failures
- Wire Bond Pull and Ball Shear Testing
- Cleanliness Testing, Solderability Testing, and Sequential Electrochemical Reduction Analysis (SERA)
- Spectroscopy Techniques
- Microsectioning and X-Ray Analysis
- Microscopy- High and Low Magnifications
- Reliability Testing and Analysis
- Integrated Circuit Failure Analysis, Delidding and Decapsulation

In the lab sessions, students will gain practical experience by working on failure analysis of samples using all the available equipment.

- Wire Bond Pull Tester, Ball Shear Tester
- Optical Microscopy, Metallograph, Scanning Electron Microscope (SEM), Energy Dispersive Spectroscopy (EDS)

- Thermal Humidity Chamber
- Thermal Cycling Chambers
- Vibration Table
- Highly Accelerated Stress Test (HAST) Chamber

Towards the end of this class, the students will look at case studies based on real-life failures experienced by vendors. The instructor will discuss the proper technique and demonstrate the methodology for determining root cause of failure.

The EMPF offers the "Failure Analysis of Electronic Assemblies" training course several times during the year. Please check the dates on the schedule at the end of this newsletter. For registration information, please contact the Registrar at 610.362.1295 or email registrar@empf.org.



Phillip Yu Senior Materials Engineer







### **COTS** Cooling

(continued from page 1)

location than heat sinks, which transfer heat to the immediately surrounding air. Figure 1-3 shows the detail of a typical cold plate system. The advantages of cold plates are that they can move large amounts of heat and that they can get the heat to a remote external location to be extracted. A drawback to a cold plate cooling system is that it requires a pump motor to move the fluid and a fan to assist in the heat exchanger in transferring the heat to the atmosphere. As usual, moving parts can create reliability concerns as well as adding the requirement for extra power consumption.

Heat pipes work using the physics of a closed loop evaporative system. This system allows the heat of the component to evaporate liquid (convert it to gas) at one end of the heat pipe, while the cool atmosphere at the other end removes heat from the gas. The liquid then condenses on the walls of the pipe and returns to the hot end, as shown in Figure 1-4. Most heat pipes contain capillaries, a screen mesh, or sintered powder on the inside of the tube walls to allow them to operate in any orientation. The ability of heat pipes to transfer heat in a closed system, while requiring no power, has made them very popular in the cooling of laptop computers.

Thermoelectric cooling is based on the operating principles of the common diode. When electric current is applied across a semi-conductor, it not only allows current to move but also allows heat to pass. The direction of the heat transfer can be controlled by the polarity of the voltage applied. A thermoelectric device is a group of "n" and "p" semiconductors connected in series to allow an active movement of heat under power. A thermoelectric cooling system cannot operate using a thermoelectric semiconductor alone. The thermoelectric device is used for its ability to force a temperature difference across its two surfaces. Typically, the thermoelectric is sandwiched between heat sinks or cold plates or a combination of the two. While thermoelectrics can force a large temperature differential over a small distance, one of the drawbacks to thermoelectric devices is the large amount of electrical power that is required to allow them to move heat. Typically, a thermoelectric device requires two watts of electrical power to move one watt of heat.

The project that the EMPF is currently working has stringent requirements from a physical and EMI perspective. The circuitry requirement dissipates over 300 watts of heat for each box during functional operation. The ambient temperature requirements for the project are  $-30^{\circ}$ C to  $+60^{\circ}$ C, and the maximum temperature of the transistor thermal plane is  $80^{\circ}$ C. The EMI concerns require a housing with no openings for air cooling. Another requirement was that four of these units need to be stacked on top of each other, so the large cooling surface area that may have been available on the top or bottom of the box could not be utilized. Available power is also a concern since the final system will be implemented in an aircraft.

A cold plate system was selected by a process of elimination based on these constraints. The constraint of EMI infiltration made a closed box the preferred housing, ruling out both natural and forced convection. The wide ambient temperature ranges and large amount of heat eliminated heat pipes as a viable solution. In considering a thermoelectric system, a maximum power draw of twice the generated heat worked out to be 300 watts x 4 units x 2, or 2.4kW. This power draw induced the EMPF to turn to a cold plate system.

This choice allows the heat to be transported away from the transistors while maintaining a closed box design. The cold plate is attached to, but electrically isolated from, heat sinks that are attached to the transistors. The heat from the transistors rises through the heat sinks, passes through an electrically isolative thermal pad to the cold plate. The cooling fluid,



Figure 1-2: Transistors connected to solid heat sinks. The unit on the left uses the aluminum plate in room temperature  $(25^{\circ}C)$  air to dissipate the added heat. The unit on the right relies on connections to exterior aluminum plates to provide a thermal conduction path at temperatures close to  $50^{\circ}C$ .

Figure 1-3: Detail of a typical cold plate system.





## **COTS** Cooling

(continued from page 7)



Figure 1-4: A heat pipe (cutaway view) is a simple device that can quickly transfer heat with almost no heat loss.

which is pumped through the cold plate, takes the heat from the transistors and transfers it to a heat exchanger mounted away from the boxes. The heat exchanger transfers the heat from the fluid to the surrounding air while fluid at ambient temperature returns to the cold plate.

The project is currently in the qualification stages for multiple military specifications. While the testing for thermal qualification has not been performed as of the writing of this edition, all calculations of the design show that the cooling using COTS components will be successful.



Walt Barger Senior Applications Engineer

## **Non-Destructive Test Methods**

(continued from page 3)

#### Automated Optical Inspection

Automated optical inspection (AOI) is used as a process tool for inspection of bare boards, solder paste deposition, component placement prior to reflow, post-reflow component conditions, solder joints, and surface anomalies on assemblies. By programming the features of a good board assembly, comparisons with subsequent assemblies can determine if they pass or fail.

#### **X-Ray Examination**

#### X-Ray Fluorescence (XRF)

XRF is used to identify composition and plating thickness for elements ranging from titanium (Ti, element 22) to uranium (U, element 92). By bombarding a sample with high energy X-rays, "secondary" (or fluorescent) X-rays can be emitted which are characteristic of the atoms present in the sample. Figure 3-4 shows an XRF spectrum that is indicative of an electroless nickel immersion gold (ENIG) surface finish over copper. Figure 3-5 shows an XRF spectrum for solder joint composed of tin-lead solder.

#### X-Ray Inspection

X-ray inspection is used to visualize assemblies by observing differences in density and composition. The denser an item, the darker it appears in the image. Some of the features that can be observed are: cracks, solder joints, traces, vias, voiding within solder joints, and wire bonds. Figure 3-6 shows a BGA component, where several groups of solder balls have bridged during the reflow process due to solder paste deposition and the thermal profile.



Figure 3-4: XRF spectrum of an electroless nickel immersion gold (ENIG) surface finish over copper, where copper (Cu), gold (Au), and nickel (Ni) were observed.

#### **Cleanliness Examination**

To determine if there are ionic contaminants present on the board assembly, there are two methods that give different levels of information: bulk ionics testing and ion chromatography. To determine if there are organic contaminants present on the assembly, Fourier transform infrared spectroscopy can be performed. A spectrum is obtained showing peak location and height which indicate what chemical functional groups (alcohol, epoxy, siloxanes) are present.





(continued from page 8)



Figure 3-5: XRF spectrum of a tin-lead solder joint, where lead (Pb) and tin (Sn) were observed.



Figure 3-6: X-ray image of a BGA component with bridging solder balls.

#### Bulk Ionics Testing

The more general method follows IPC-TM-650 2.3.25C, Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract (ROSE)<sup>1</sup>, in which a sample is immersed in an isothermal bath (at 35°C) containing a 3 to 1 solution of isopropyl alcohol to deionized water. Ionic contaminants extracted from the sample pass through a conductivity cell which continuously measures the conductivity of the solution. The conductivity values are integrated over the time of the extraction. The ionic material then passes through a deionization

column before being recirculated back into the test chamber. As the ionic materials are extracted from the assemblies, the conductivity (and hence resistivity) of the solution will change dynamically until nearly all of the extractable ionic material has been removed.

Results from dynamic extraction by Ionograph are reported in micrograms of sodium chloride (NaCl) equivalent per square inch. For assemblies soldered using rosin based fluxes, the ionic cleanliness requirement per J-STD-001D is a maximum of 10.06  $\mu$ g NaCl equivalent/in<sup>2</sup> (1.56  $\mu$ g NaCl equivalent/cm<sup>2</sup>). There is no industry standard for acceptable bulk ionic levels, but it is better to have as low a value as possible. The EMPF recommends Ionograph results to not exceed a level of 2 to 3  $\mu$ g NaCl equivalent/in<sup>2</sup>.

#### Ion Chromatography

The more specific method of ionic contaminant analysis is IPC-TM-650 2.3.28A, Ionic Analysis of Circuit Boards, Ion Chromatography Method<sup>2</sup>, in which the samples are sealed in a Kapak bag with a 3 to 1 solution of isopropyl alcohol to water and heated in an 80 °C water bath for 1 hour to extract any ionic residues. The extract solution is analyzed against known standards to confirm the presence of and quantify each of the following anions: fluoride, chloride, bromide, nitrate, phosphate, and sulfate in units of  $\mu$ g/mL. The surface area is calculated from the board dimensions and the final results are reported in  $\mu$ g/in<sup>2</sup>.

The EMPF's maximum recommended amounts of fluoride, chloride, bromide, nitrate, and sulfate for bare boards are 2, 4, 5, 1, and 3  $\mu$ g/in<sup>2</sup>, respectively. The recommended levels of ionic contamination for populated assemblies will depend upon the application. However, for typical component packages on FR-4 or a like substrate, the maximum recommended amounts of fluoride, chloride, bromide, nitrate, and sulfate are 2, 9, 15, 1 and 10  $\mu$ g/in<sup>2</sup>, respectively. Both sets of acceptance criteria were developed from experience and in conjunction with industry leaders.

An example of an ion chromatograph is shown in Figure 3-7. The anions in solution are separated from one another by their different rates of interaction with the quaternary ammonium groups in an ion-exchange column. A set of standards is run with the samples to compare elusion times (how long it takes for an anion to leave the ion-exchange column) and corresponds to the identity of the anion. The peaks correspond to different anions passing through an electrochemical detector, which measures changes in conductivity resulting from the flow of ions in solution when moving through an electric field. The level of conductivity is directly proportional to the concentration of the anion, which is calculated by integrating the area under the peaks.

#### Fourier Transform Infrared Spectroscopy

Fourier transform infrared (FTIR) spectroscopy is used to identify organic materials (those containing mostly carbon) such as: cleaning chemicals, rosins, and polymers used in conformal coatings. FTIR spectroscopy is a technique in which infrared energy is used to excite fundamental vibrational and associated rotational-vibrational modes of continued on page 10





molecules in the mid-infrared, approximately 4000 to 400 cm<sup>-1</sup>. These vibrational modes correspond to molecular structures. Attenuated Total Reflectance (ATR) is a technique used with FTIR, which allows liquid and solid samples to be studied directly without further preparation. In ATR-FTIR, an infrared beam is directed through an optically dense crystal at a certain angle and internally reflects through the crystal, producing evanescent waves. When the crystal is pressed against an infrared active material, the infrared radiation from the evanescent waves penetrates typically one to four micrometers into the sample.



Figure 3-7: Example of an ion chromatograph showing the presence and separation of the anions: fluoride (F), chloride (Cl), bromide (Br), nitrate (NO<sub>3</sub>), phosphate (PO<sub>i</sub><sup>2</sup>), and sulfate (SO<sub>i</sub><sup>2</sup>).



Figure 3-8: FTIR spectra for an unknown residue from a board assembly (top, red) compared to a known adhesive compound (bottom, blue).

Figure 3-8 shows an FTIR spectrum of an unknown residue rinsed off a board assembly compared to that of a known adhesive compound. The residue was contributing to the poor adhesion of a conformal coating to this assembly.

#### **Mechanical Examination**

#### Non-Destructive Wire Bond Pull Test

Method 2023.5 of MIL-STD-883<sup>3</sup> provides for a Non-Destructive Bond Pull, where an applied stress (measured in grams force (gf) pull) is used to reveal non-acceptable wire bonds while avoiding damage to acceptable wire bonds in a package. This test is intended for "Class S" parts or parts intended for use in the high reliability space flight community<sup>4</sup>. Any bond failures are unacceptable, but based on the program requirements, rework and retest may be acceptable. Table 3-1 lists the pull forces for a set of standard wire sizes.

Al and Au Wire Diameter (inches)	Pull Force (gf) Al	Pull Force (gf) Au
0.0007	1.2	1.6
0.0010	2.0	2.4
0.00125	2.5	3.2
0.0013	2.5	3.2
0.0015	3.0	4.0
0.0030	9.5	12.0

Table 3-1: Non-Destructive Pull Forces

There are conditions for which this test may not be applicable, such as having a high pin count of 84 or more external terminations and small bonding wire pitch at the package post of less than or equal to 12 mils (304.8 µm). Alternative procedures are given to evaluate the wire bonds, such as: review of manufacture quality records and raw material control, a thermal mechanical analysis of the package and the bonds over time and with temperature cycling, and a 100% visual inspection of all bonds. For packages with gold plated posts, a bake test at 300°C for one hour in air or inert atmosphere is performed to test for contamination anomalies in the plating. This bake test calls for 45 bond pulls to destruction per method 2011 of MIL-STD-883 and falls into the realm of destructive testing.

#### Summary

Non-destructive testing can provide valuable information as to the root cause of failures that can occur in electronics manufacturing. The EMPF facilities are well equipped to assist with non-destructive testing using all of these techniques, along with the skilled staff to provide interpretation of the data, and provide the appropriate recommendations to remedy the conditions leading to failure.





(continued from page 10)

- "Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract - 2/01." IPC-TM-650 2.3.25C <http://www.ipc.org/4.0 Knowledge/4.1 Standards/test/2-3 2-3-25c.pdf>
- <sup>2</sup> "Ionic Analysis of Circuit Boards, Ion Chromatography Method 5/04." IPC-TM-650 2.3.28A. <http://www.ipc.org/4.0 Knowledge/4.1 Standards/test/2.3.28A.pdf>
- 3 "Test Method Standards, Microcircuits." MIL-STD-883. <http://www.dscc.dla.mil/Programs/MilSpec/listdocs.asp?BasicDoc=MIL-STD-883>
- 4 "Assurance Issues Related to Electronic Wire Bonds." NASA Goddard Space Flight Center. <http://nepp.nasa.gov/wirebond/>



Sean Clancy, Ph.D. Research Associate/Chemist

## **Manufacturer's Corner: Metcal**

(continued from page 5)

adjustable angle cradle that allows operators to select and lock the angle for tool placement in the holder to meet their preference to increase ergonomics and productivity.

For more information related to this article, or to schedule a demonstration of Metcal's MX-5000 soldering/desoldering system located at the EMPF, contact Ken Friedman at 610.362.1200, extension 279 or via email at kfriedman@aciusa.org.



Ken Friedman EAB Coordinator

## **Upcoming Courses**

### **IPC** A-610

October 19-22 Certification October 26-27 Recertification

Achieve the highest quality and most cost-effective productivity by knowing how to correctly apply the IPC A-610 acceptability criteria.

### Failure Analysis and Reliability Testing

#### November 16-18

This course features both lecture and lab sessions. Learn the latest analytical methods to troubleshoot from manufacturing and laboratory perspectives. Content includes the latest information on lead-free solder, x-ray fluorescence, RF plasma etching and microprobing of integrated circuits.

### **Boot Camp**

November 2-6 Boot Camp A November 9-13 Boot Camp B

Designed to provide electronics manufacturing personnel with intense, hands-on training in every aspect of the electronics manufacturing process. Experience setting up screen printers, programming and placing components using automated equipment, profiling reflow ovens and wave soldering machines, and selecting various types of cleaning processes. Engage in decision-making exercises relating to process options including flux considerations, cover process control tools, troubleshooting and cause/effect.

**CONTACT THE REGISTRAR VIA:** phone at 610.362.1295, email at registrar@empf.org or online at www.aciusa.org/courses





## ACI Technologies, Inc.

National Electronics Manufacturing Technology Center of Excellence **Class Schedule for the Calendar Year 2009** 





**Contact the Registrar** for course information and pricing: 610.362.1295 FAX: 610.362.1289 registrar@empf.org

**Contact the EMPF Helpline for** electronics manufacturing assistance: 610.362.1320 helpline@empf.org

**Custom courses** and on-site training are available

**Conveniently located** next to the **Philadelphia International Airport** 

# ISO 9001:2000 CERTIFIED

#### Electronics Manufacturing

**Boot Camp A** January 26-30 March 23-27 June 15-19 August 17-21 November 2-6

**Boot Camp B** February 2-6 March 30 - April 3 June 22-26 August 24-28 November 9-13

### **CIS/Operator**

IPC J-STD-001 Call for Availability

IPC 7711/7721 Call for Availability

**IPC A-610** Call for Availability

#### IPC/WHMA-A-620A **CIS** Certification March 16-18 May 4-6

August 10-12 October 5-7 December 14-16

#### **IPC CIT Challenge Test**

January 23 February 27 March 27 April 24 May 29 July 31 August 21 September 25 October 23 December 11 Call for Additional Availabilities

**IPC Certifications CIT/Instructor** 

#### IPC J-STD-001 **CIT Certification** January 5-9 February 9-13 March 9-13 April 13-17 May 18-22 June 22-26 July 6-10 August 10-14 September 14-16 October 12-16 November 2-6

December 14-18 IPC J-STD-001

### **CIT Recertification**

January 14-15 March 25-26 April 29-30 June 17-18 August 26-27 September 23-24 October 28-29

**IPC A-610 CIT Certification** February 23-26

March 16-19 June 8-11 July 6-9 August 17-20 October 19-22 December 7-10

**IPC A-610 CIT Recertification** January 12-13 March 23-24

April 27-28 June 15-16 July 27-28 August 24-25 September 21-22 October 26-27 November 30 -December 1 **IPC A-600 CIT** Certification January 20-22 April 6-8 July 20-22 August 31 - September 2 November 16-18

IPC 7711/7721 **CIT Certification** March 2-6 June 1-5 August 3-7 November 9-13

### IPC 7711/7721

**CIT Recertification** February 23-24 May 4-5 July 13-14 September 28-29

#### **High Reliability** Addendum

**IPC J-STD-001 DS CIT Certification** January 16 May 1 August 28 October 30 December 4

### Skills

**Chip Scale** Manufacturing March 2-4 May 13-15 August 3-5 December 2-4

**BGA Manufacturing**, **Inspection**, Rework January 5-6

April 20-21 July 13-14 September 14-15 December 7-8

#### Continuing Professional Advancement in Electronics Manufacturing

Lead Free Manufacturing March 9-10 May 11-12 July 27-28 September 16-17 November 30 -December 1

**Design for** 

Manufacture January 12-13 April 27-28 July 20-21 September 21-22

#### **Failure Analysis and Reliability Testing** February 9-11

April 6-8 June 29 - July 1 August 31 - September 2 November 16-18

